

GM3(B) Pacino Intel Discrete & UMA Block Diagram

VER : 3A

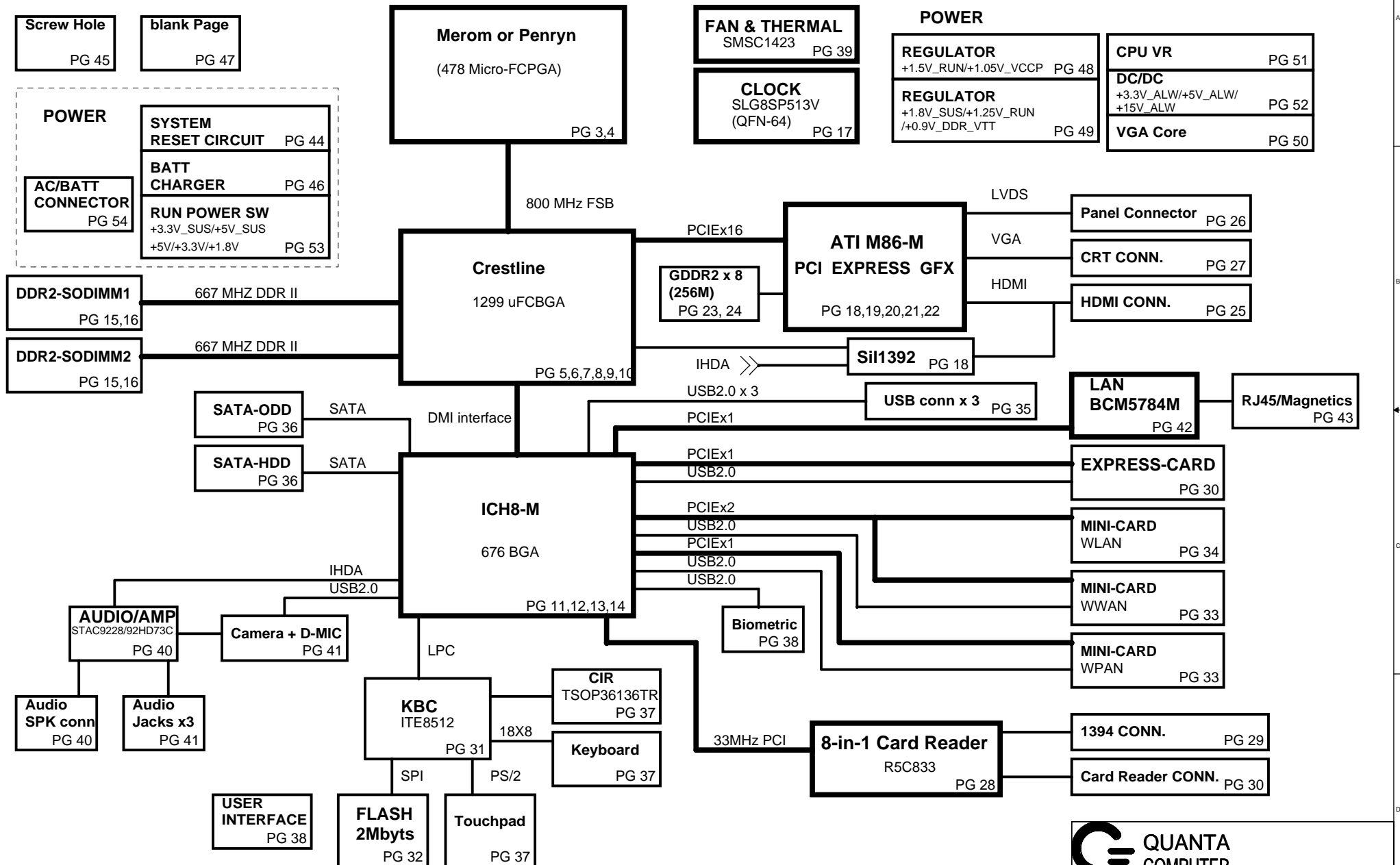


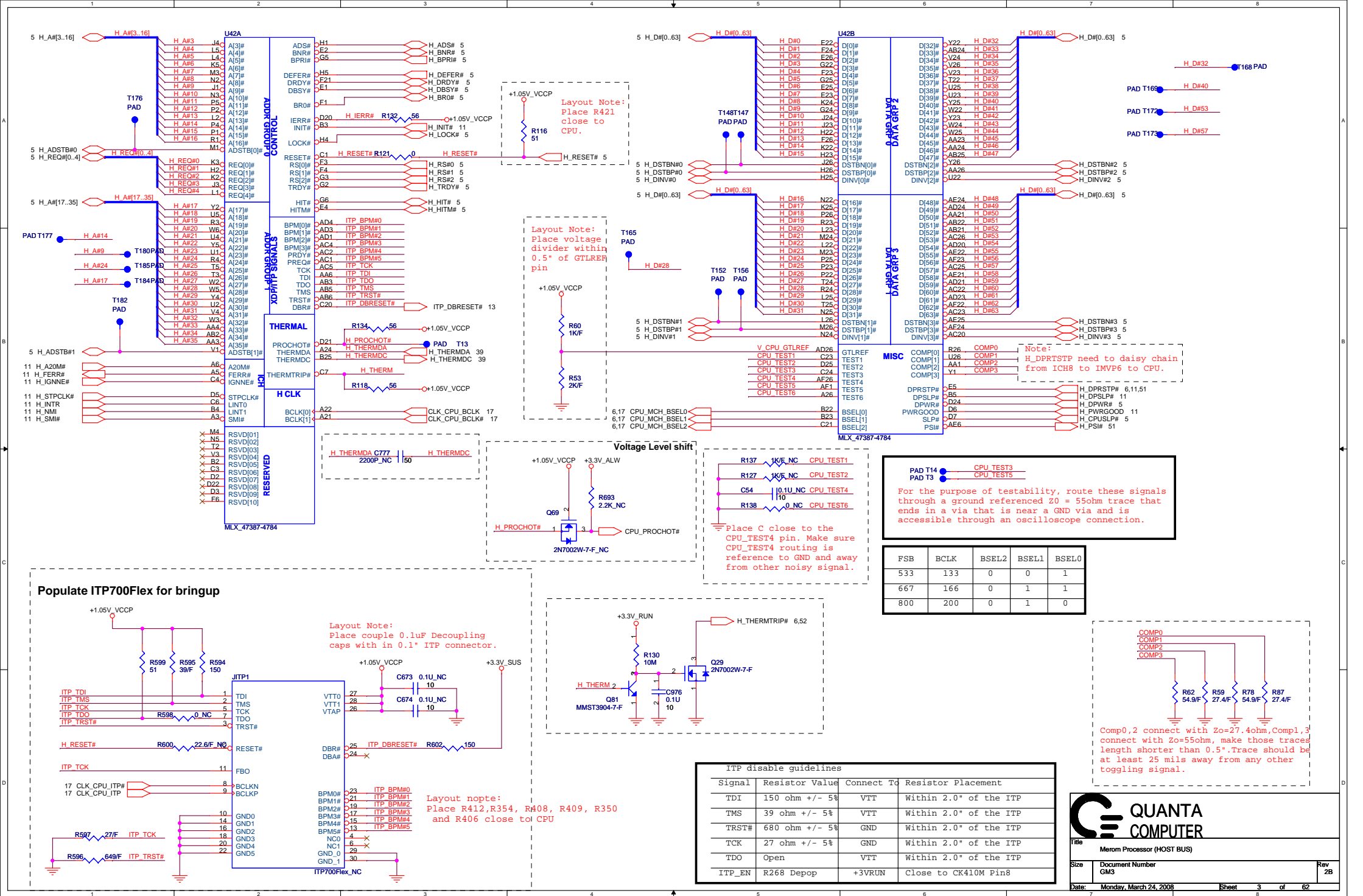
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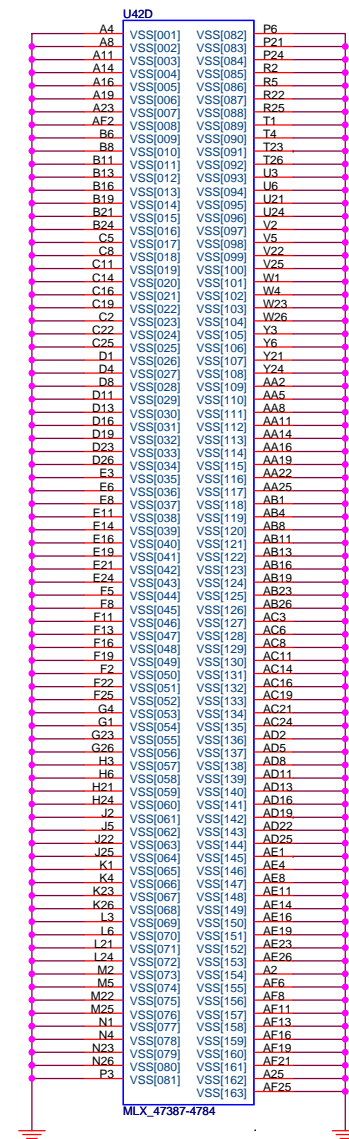
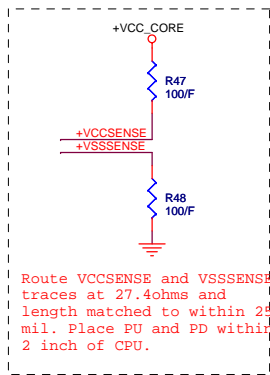
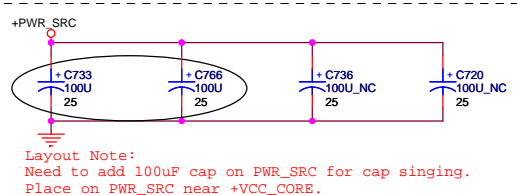
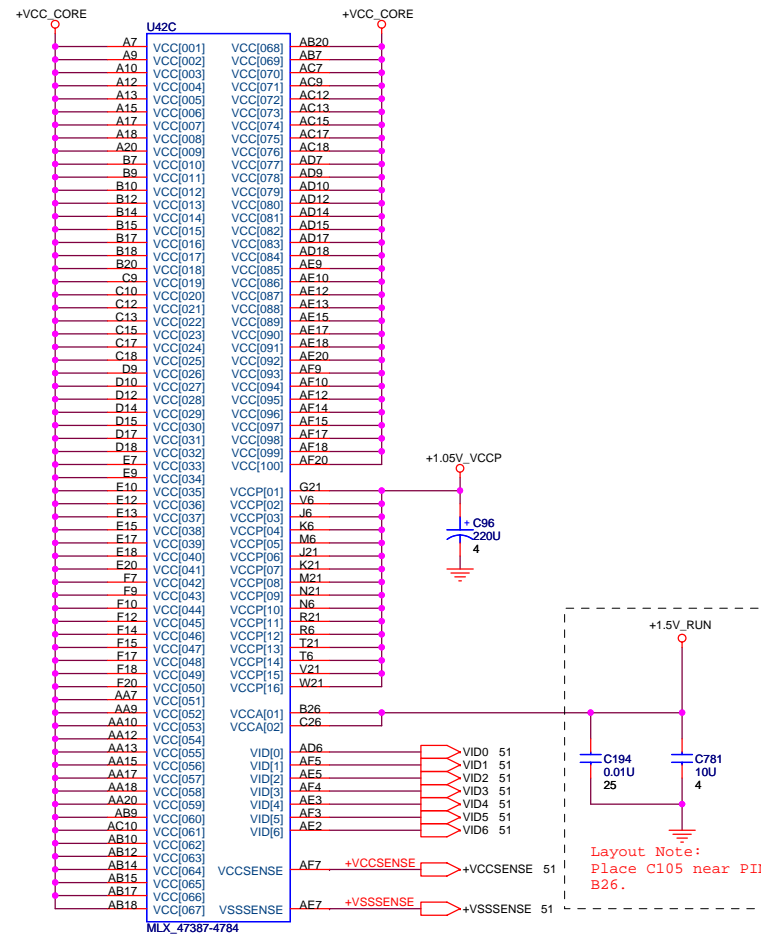
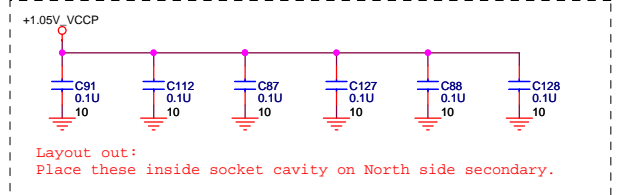
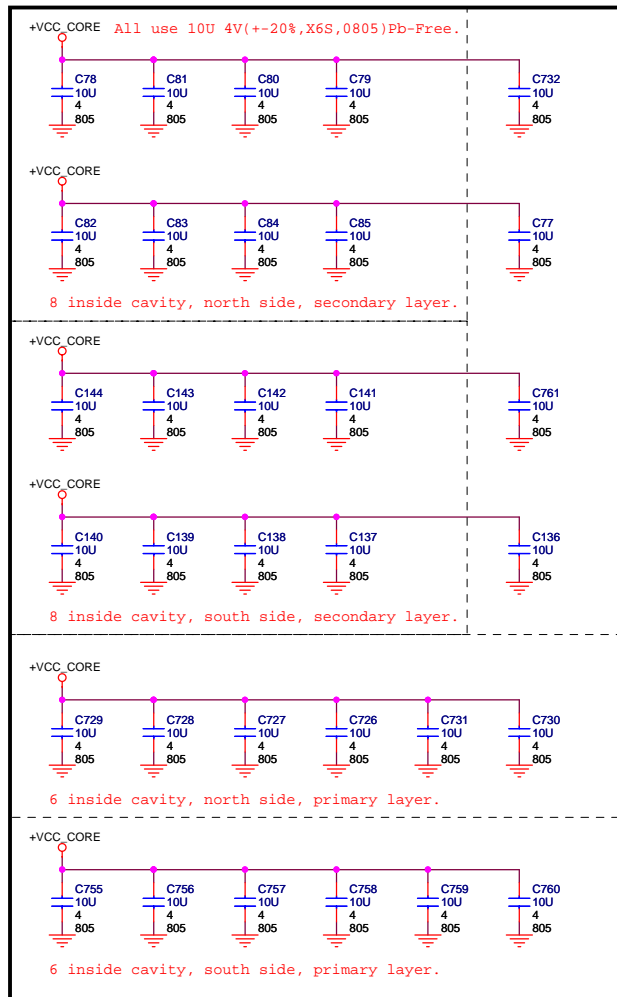
| PAGE | DESCRIPTION |
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| 5-10 | Crestline |
| 11-14 | ICH8M |
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| 17 | Clock Generator |
| 18-24 | VGA |
| 25 | HDMI |
| 26 | LCD connector |
| 27 | CRT |
| 28 | Card reader PCI interface |
| 29 | Card reader & 1394 |
| 30 | Express card & card reader conn. |
| 31 | SIO |
| 32 | Flash/RTC |
| 33 | WWAN/WPAN |
| 34 | WLAN |
| 35 | USB port |
| 36 | SATA HDD & ODD |
| 37 | TP/KB/MB/CIR |
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| 51 | CPU_ISL6266 (2phase) |
| 52 | D/D ISL6237 3.3V/5V |
| 53 | RUN Power Switch |
| 54 | DCIN,Batt |
| 55 | EMI CAP |
| 56 | SMBUS BLOCK |
| 57 | Power statu & Block diagram |

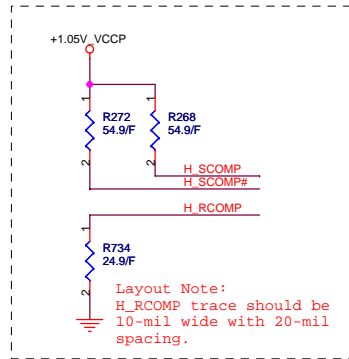
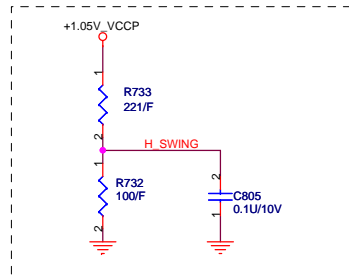
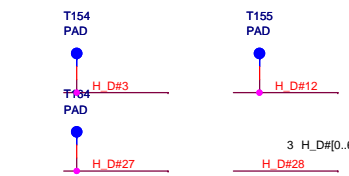
Power States

| POWER PLANE | VOLTAGE | PAGE | DESCRIPTION | CONTROL SIGNAL | ACTIVE IN |
|---------------|-------------|-------------------------------------------------------------------------------|--------------------------|-----------------------|-----------|
| +PWR_SRC | 10V~+19V | 4,26,32,34,48,49,50,51,52,55 | MAIN POWER | | S0~S5 |
| +RTC_CELL | +3.0V~+3.3V | 11,14,31,32 | RTC | | S0~S5 |
| +3.3V_ALW | +3.3V | 3,13,26,31,32,34,36,37,38,44,46,49,52,53,54 | 8051 POWER | ALWON | S0~S5 |
| +5V_ALW | +5V | 35,36,46,48,49,52,53,54 | LCD/CHARGE POWER | ALWON | S0~S5 |
| +15V_ALW | +15V | 26,36,37,52,53 | LARGE POWER | +5V_ALW | S0~S5 |
| +3.3V_LAN | +3.3V | 42,43 | LAN POWER | AUX_ON | |
| +5V_SUS | +5V | 14,38,50,51,53 | SLP_S5# CTRLD POWER | SUS_ON | |
| +3.3V_SUS | +3.3V | 3,11,12,13,14,20,30,37,38,43,48,49,50,51,53 | SLP_S5# CTRLD POWER | 3.3V_SUS_ON | |
| +1.8V_SUS | +1.8V | 6,8,9,15,48,49,50,53,55 | SODIMM POWER | DDR_ON | |
| +0.9V_DDR_VTT | +0.9V | 16,49,53 | SODIMM POWER | 0.9V_DDR_VTT_ON | |
| +5V_RUN | +5V | 14,20,25,27,36,37,38,39,40,41,53 | SLP_S3# CTRLD POWER | RUN_ON | |
| +3.3V_RUN | +3.3V | 6,8,9,11,12,13,14,15,17,19,20,22,25,26,27,28,30,33,34,36,38,39,40,41,42,53,55 | SLP_S3# CTRLD POWER | 3.3V_RUN_ON | |
| +1.8V_RUN | +1.8V | 19,20,21,22,23,24,25,38,53 | SDVO POWER | RUN_ON | |
| +1.5V_RUN | +1.5V | 4,9,14,30,33,34,48,,53,55 | CALISTOGA/ICH8 POWER | 1.5V_RUN_ON | |
| +1.25V_RUN | +1.25V | 6,9,14,49,53 | CALISTOGA/ICH8 POWER | 1.25V_RUN_ON | |
| +1.05V_VCCP | +1.05V | 3,4,5,6,8,9,11,14,37,48,55 | CPU/CALISTOGA/ICH8 POWER | 1.05V_RUN_ON | |
| +VCC_CORE | +0.7V~+1.5V | 4,51 | CPU CORE POWER | IMVP_VR_ON | |
| +LCDVCC | +3.3V | 26 | LCD Power | LCDVCC_TST_EN & ENVDD | |
| +5V_MOD | +5V | 36 | Module Power | MODC_EN# | |
| +5V_HDD | +5V | 36 | HDD Power | HDDC_EN# | |
| +5V_ALW2 | +5V | 37,38,52,53 | LED power source | LDO output | |
| | | | | | |

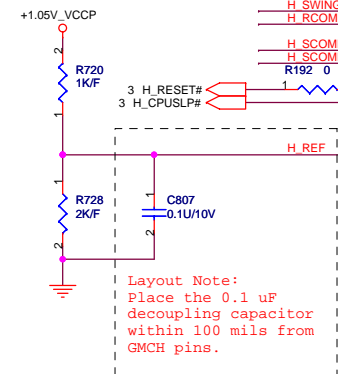
| GND PLANE | PAGE | DESCRIPTION |
|----------------|------|-------------|
| ⏏ 8731AGND | 46 | |
| ⏏ AGND_0.9V | 49 | |
| ⏏ AGND_DC/DC | 52 | |
| ⏏ AGND_DC2 | 48 | |
| ⏏ AGND_DDR | 49 | |
| ⏏ AGND_ISL6260 | 51 | |
| ⏏ GND | ALL | |







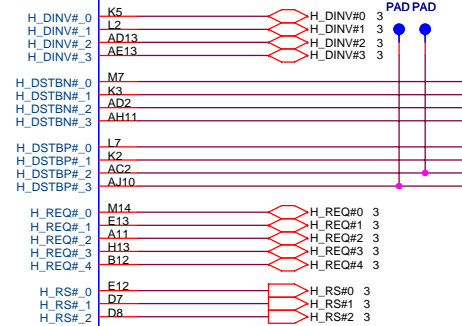
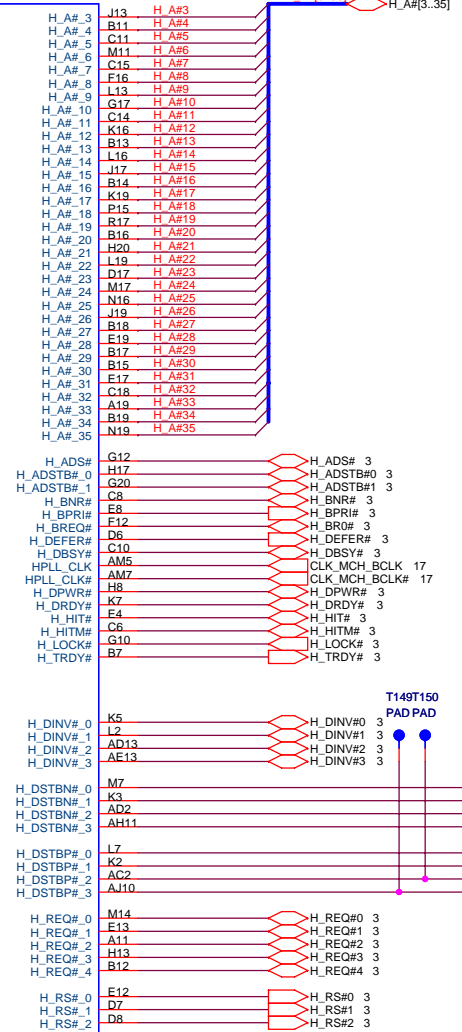
Layout Note:
H_RCOMP trace should be
10-mil wide with 20-mil
spacing.



Layout Note:
Place the 0.1 uF
decoupling capacitor
within 100 mils from
GMCH pins.

| | | |
|--------|------|---------|
| H_D#0 | E2 | H_D#_0 |
| H_D#1 | G2 | H_D#_1 |
| H_D#2 | G7 | H_D#_2 |
| H_D#3 | M6 | H_D#_3 |
| H_D#4 | H7 | H_D#_4 |
| H_D#5 | H3 | H_D#_5 |
| H_D#6 | G4 | H_D#_6 |
| H_D#7 | F3 | H_D#_7 |
| H_D#8 | N8 | H_D#_8 |
| H_D#9 | H2 | H_D#_9 |
| H_D#10 | M10 | H_D#_10 |
| H_D#11 | N12 | H_D#_11 |
| H_D#12 | N9 | H_D#_12 |
| H_D#13 | H5 | H_D#_13 |
| H_D#14 | P13 | H_D#_14 |
| H_D#15 | K9 | H_D#_15 |
| H_D#16 | M2 | H_D#_16 |
| H_D#17 | W10 | H_D#_17 |
| H_D#18 | Y8 | H_D#_18 |
| H_D#19 | V4 | H_D#_19 |
| H_D#20 | M3 | H_D#_20 |
| H_D#21 | J1 | H_D#_21 |
| H_D#22 | N5 | H_D#_22 |
| H_D#23 | N3 | H_D#_23 |
| H_D#24 | W6 | H_D#_24 |
| H_D#25 | W9 | H_D#_25 |
| H_D#26 | N2 | H_D#_26 |
| H_D#27 | Y7 | H_D#_27 |
| H_D#28 | V9 | H_D#_28 |
| H_D#29 | P4 | H_D#_29 |
| H_D#30 | W3 | H_D#_30 |
| H_D#31 | N1 | H_D#_31 |
| H_D#32 | AD12 | H_D#_32 |
| H_D#33 | AE3 | H_D#_33 |
| H_D#34 | AD8 | H_D#_34 |
| H_D#35 | AC9 | H_D#_35 |
| H_D#36 | AC7 | H_D#_36 |
| H_D#37 | AC14 | H_D#_37 |
| H_D#38 | AD11 | H_D#_38 |
| H_D#39 | AC11 | H_D#_39 |
| H_D#40 | AB2 | H_D#_40 |
| H_D#41 | AD7 | H_D#_41 |
| H_D#42 | AB1 | H_D#_42 |
| H_D#43 | Y3 | H_D#_43 |
| H_D#44 | AC6 | H_D#_44 |
| H_D#45 | AE2 | H_D#_45 |
| H_D#46 | AC5 | H_D#_46 |
| H_D#47 | AG3 | H_D#_47 |
| H_D#48 | AJ9 | H_D#_48 |
| H_D#49 | AH8 | H_D#_49 |
| H_D#50 | AJ14 | H_D#_50 |
| H_D#51 | AE9 | H_D#_51 |
| H_D#52 | AE11 | H_D#_52 |
| H_D#53 | AH12 | H_D#_53 |
| H_D#54 | AJ5 | H_D#_54 |
| H_D#55 | AH5 | H_D#_55 |
| H_D#56 | AJ6 | H_D#_56 |
| H_D#57 | AE7 | H_D#_57 |
| H_D#58 | AJ7 | H_D#_58 |
| H_D#59 | AJ2 | H_D#_59 |
| H_D#60 | AE5 | H_D#_60 |
| H_D#61 | AJ3 | H_D#_61 |
| H_D#62 | AH2 | H_D#_62 |
| H_D#63 | AH13 | H_D#_63 |

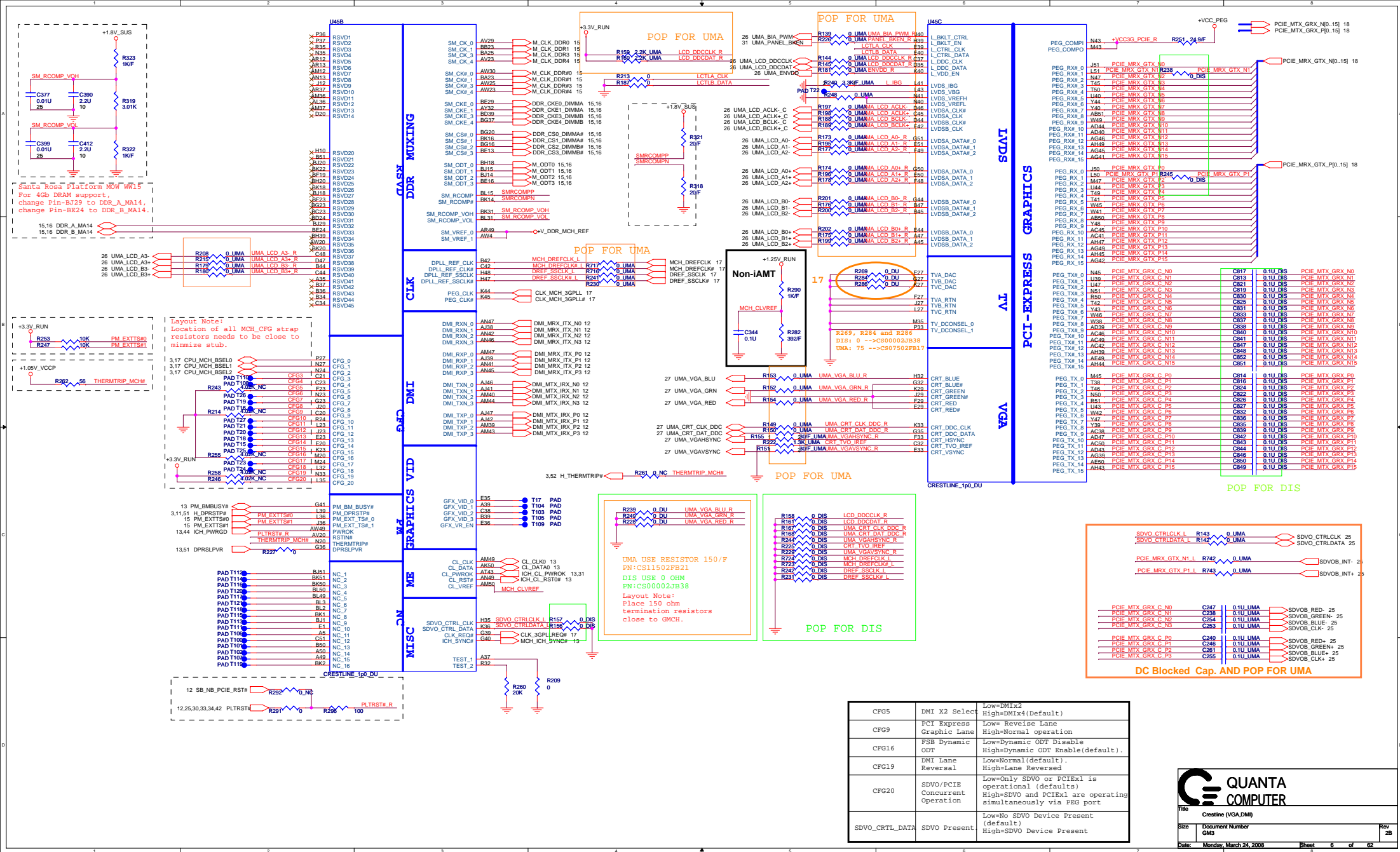
HOST



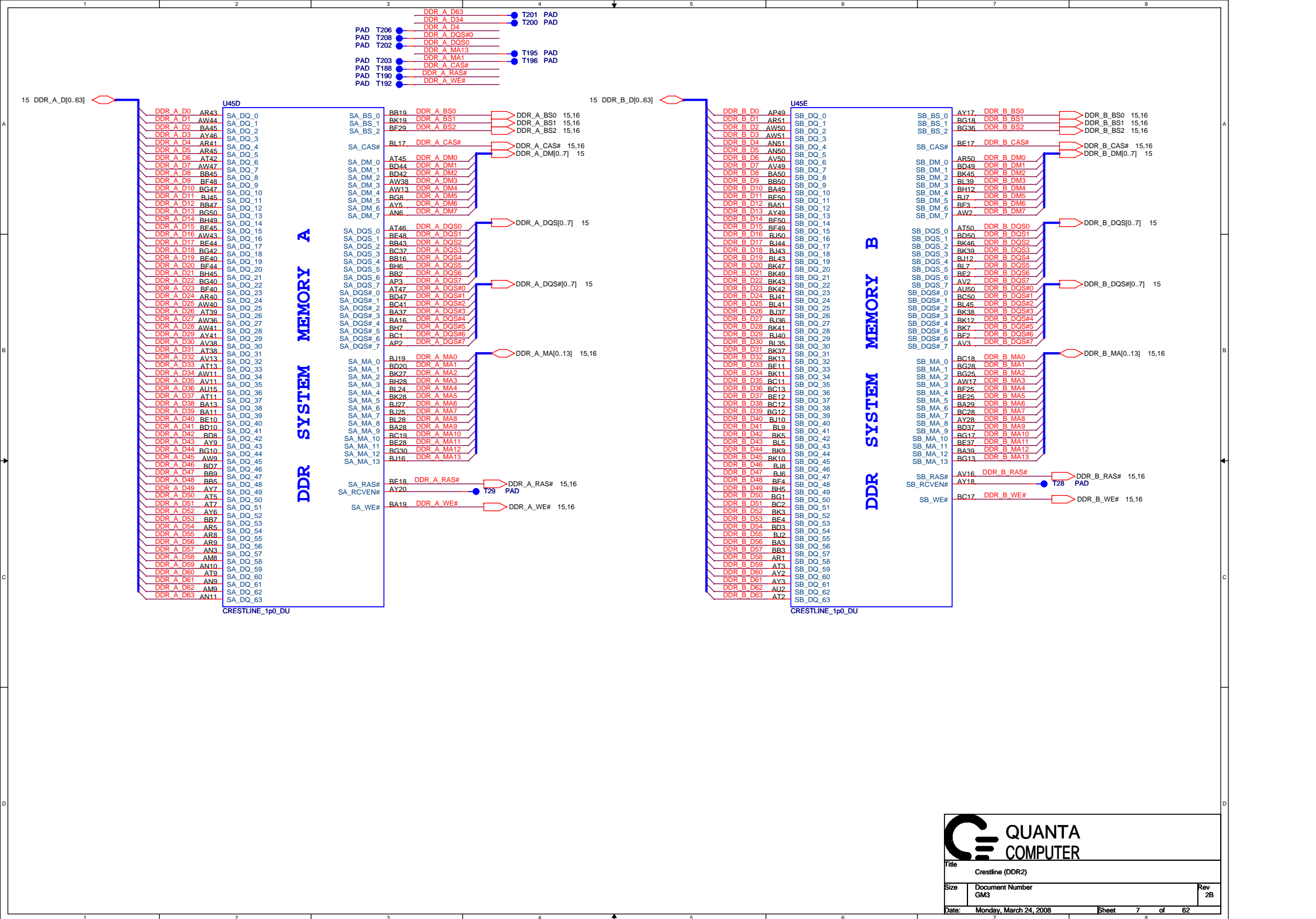
U45 QCI PN
DIS
AJSLA5U0T11
UMA
AJSLA5T0T13

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| | | |
|---------------------------------|------------------------|-----------|
| Title Crestline (HOST) | | |
| Size GM3 | Document Number GM3 | Rev 2B |
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| | | |
|----------------|--------------------------------------|--------------------------------------------------------------------------------------------------------------------------|
| CFG5 | DMI X2 Select | Low=DMIx2 High=DMIx4(Default) |
| CFG9 | PCI Express Graphic Lane | Low= Reverse Lane High=Normal operation |
| CFG16 | FSB Dynamic ODT | Low=Dynamic ODT Disable High=Dynamic ODT Enable(default). |
| CFG19 | DMI Lane Reverse | Low=Normal (default) . High=Lane Reversed |
| CFG20 | SDVO/PCIe Concurrent Operation | Low=Only SDVO or PCIeI1 is operational (default) High=SDVO and PCIeI1 are operating simultaneously via PEG port |
| SDVO_CTRL_DATA | SDVO Present | Low=No SDVO Device Present (default) High=SDVO Device Present |





Size

Document Number

Rev

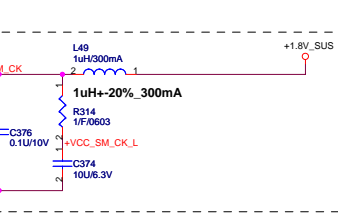
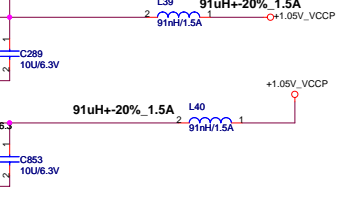
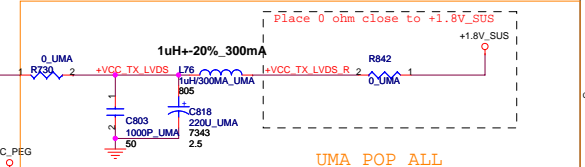
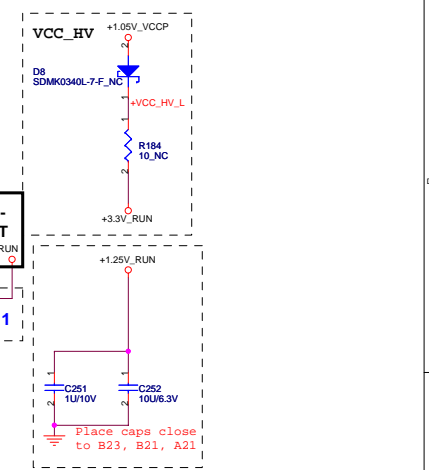
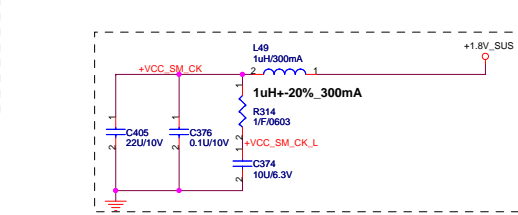
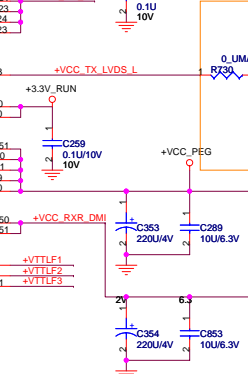
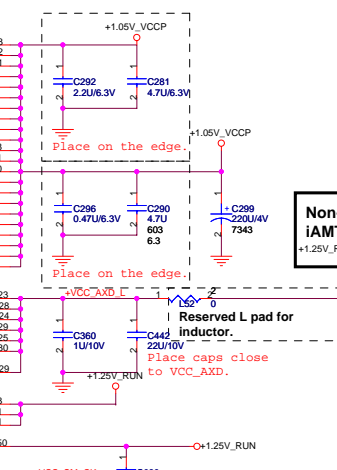
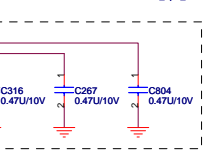
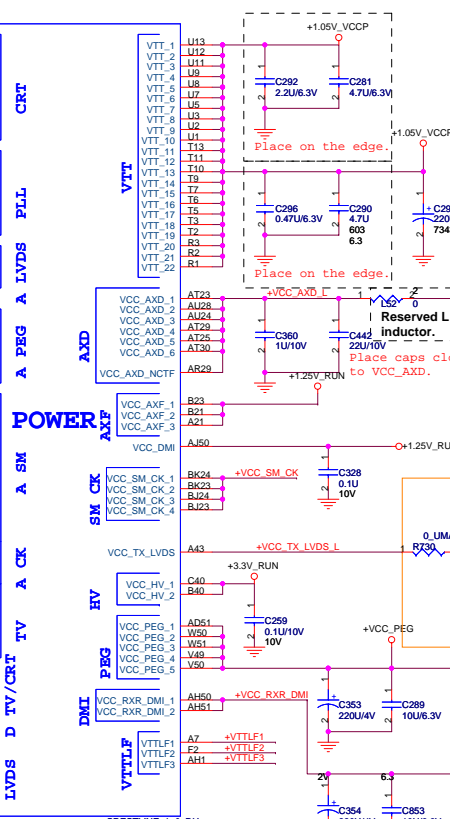
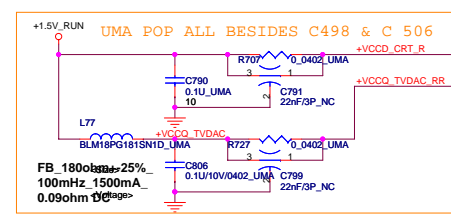
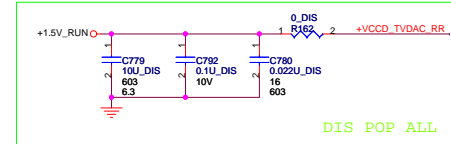
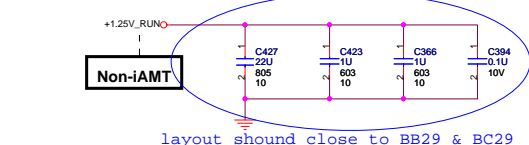
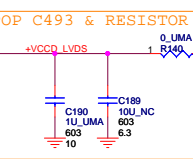
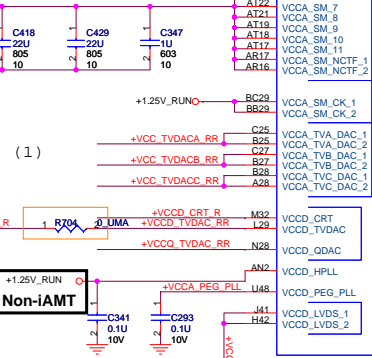
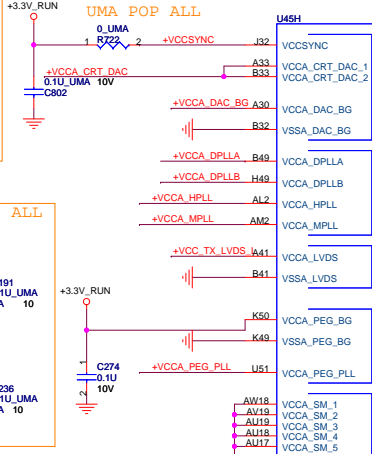
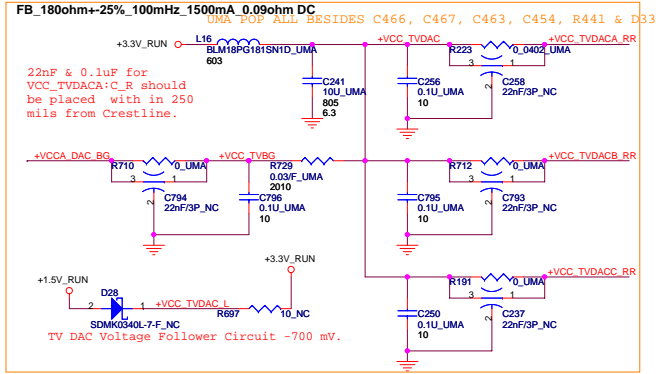
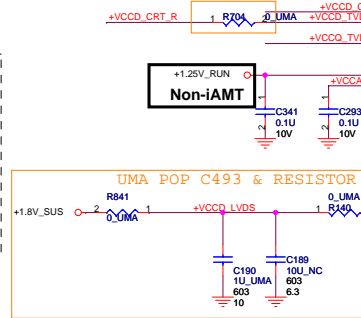
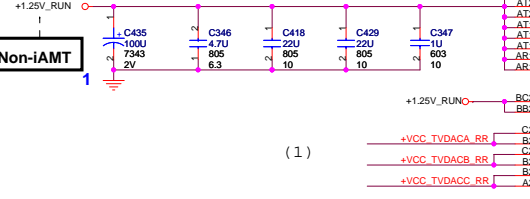
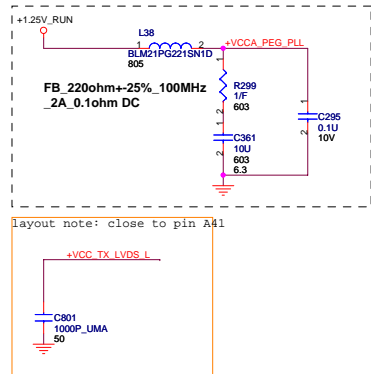
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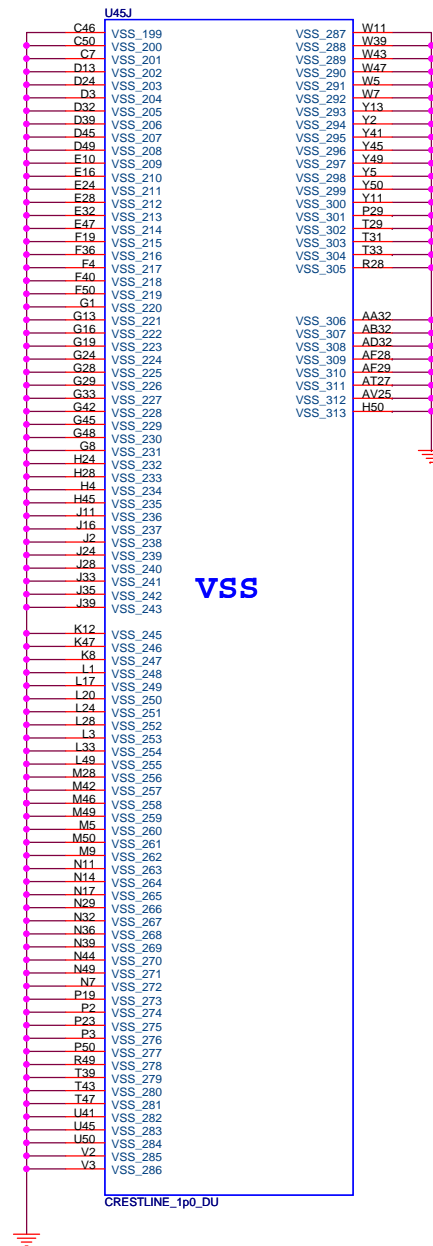
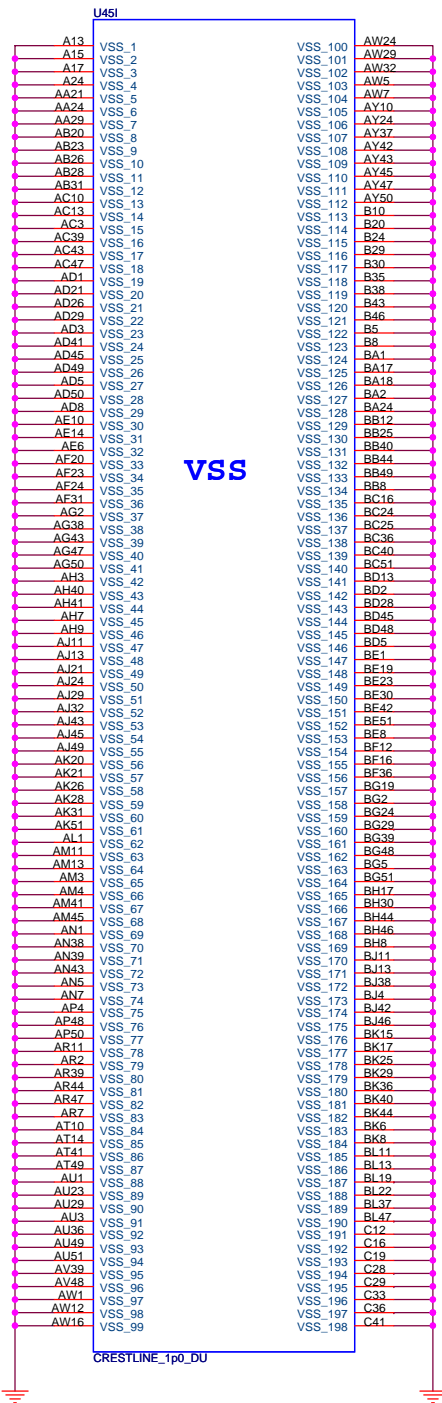
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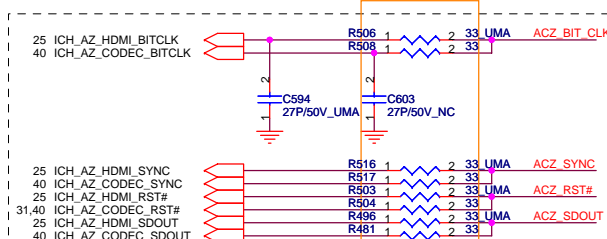
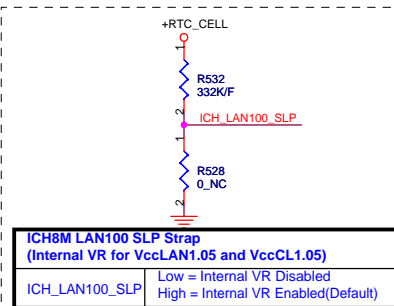
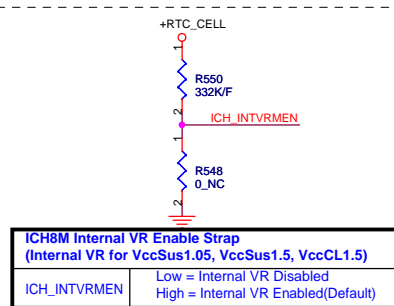
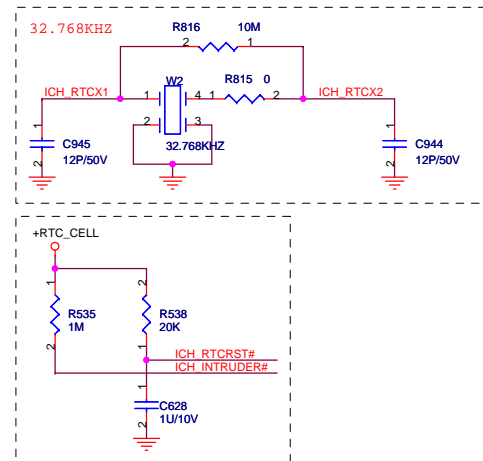
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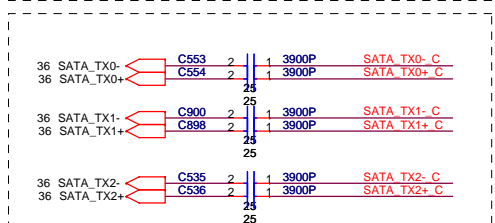
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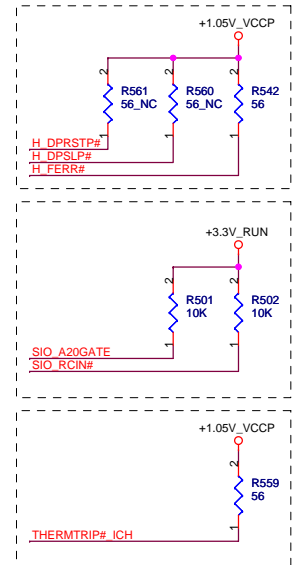
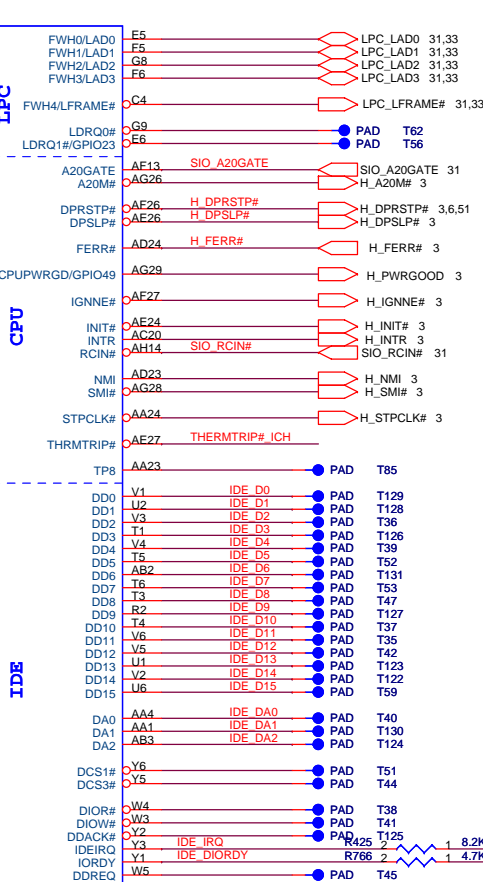
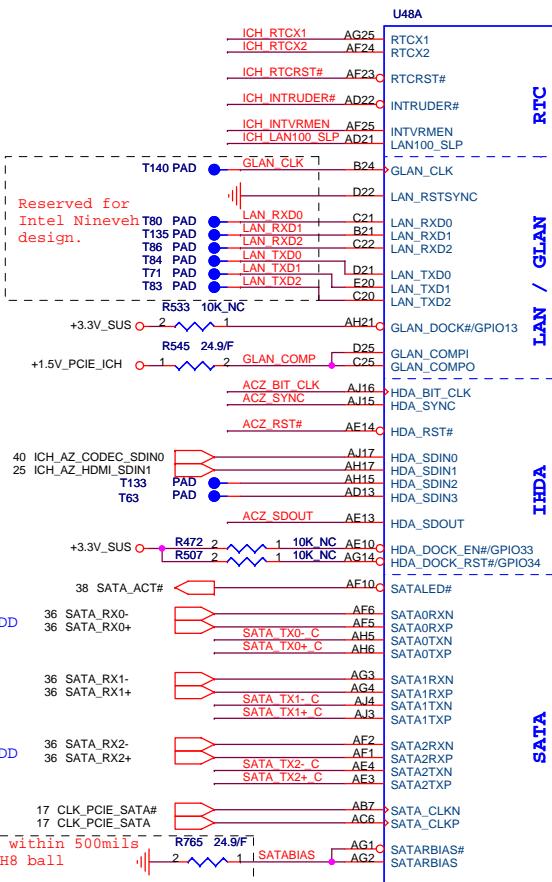




Place all series terms close to ICH8 except for SDIN input lines, which should be close to source. Placement of R603, R600, R607 & R612 should equal distance to the T split trace point as R604, R599, R606 & R608 respectively. Basically, keep the same distance from T for all series termination resistors.



Distance between the ICH-8 M and cap on the "P" signal should be identical distance between the ICH-8 M and cap on the "N" signal for same pair.



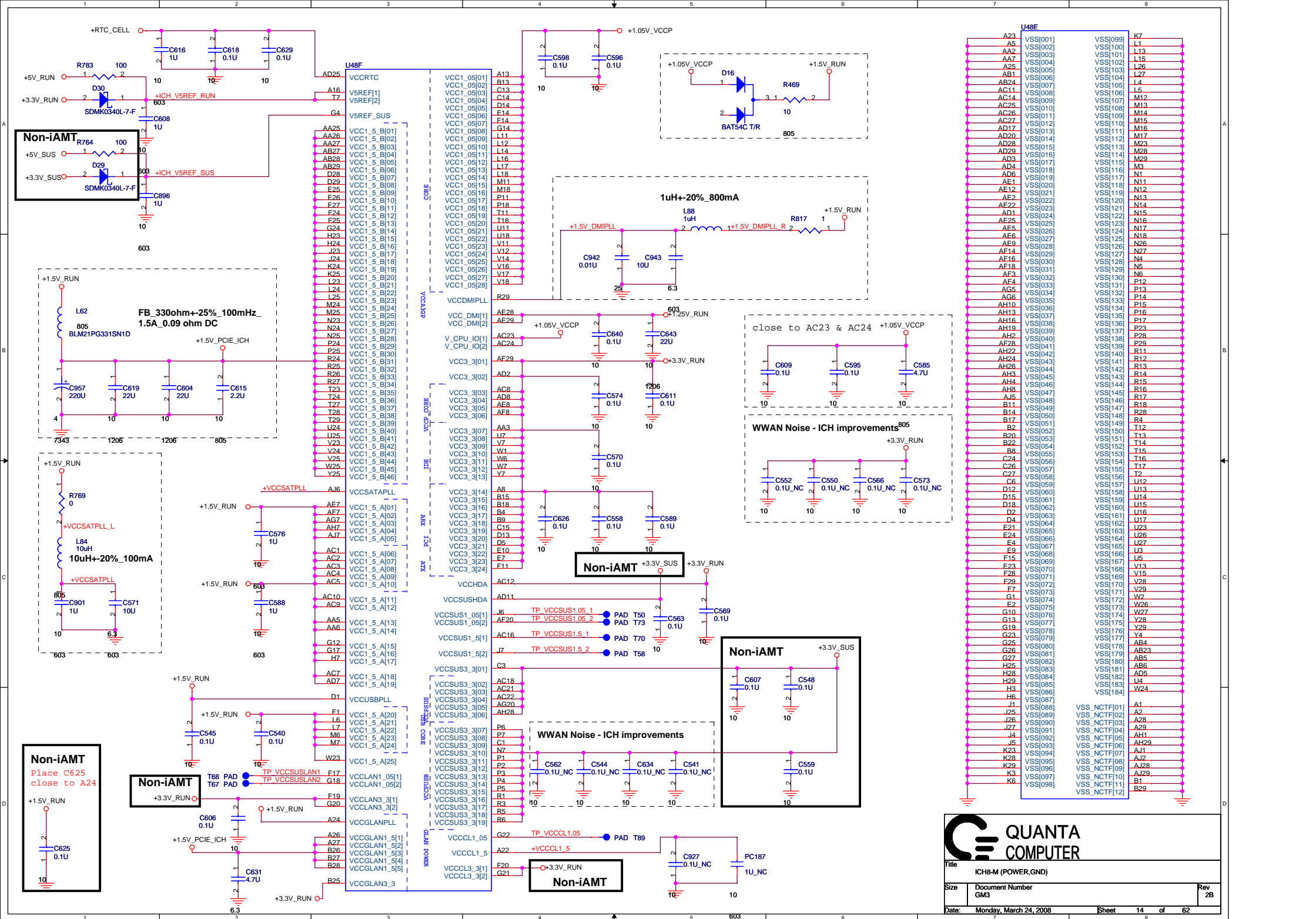
| XOR Chain Entrance Strap | | |
|--------------------------|-----------|----------------------------|
| ICH_RSVD | HDA_SDOUT | Description |
| 0 | 0 | RSVD |
| 0 | 1 | Enter XOR Chain |
| 1 | 0 | Normal Operation (Default) |
| 1 | 1 | Set PCIE port config bit 1 |

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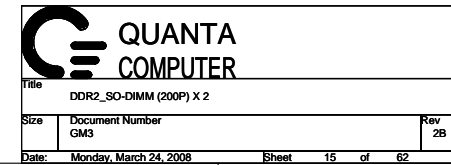
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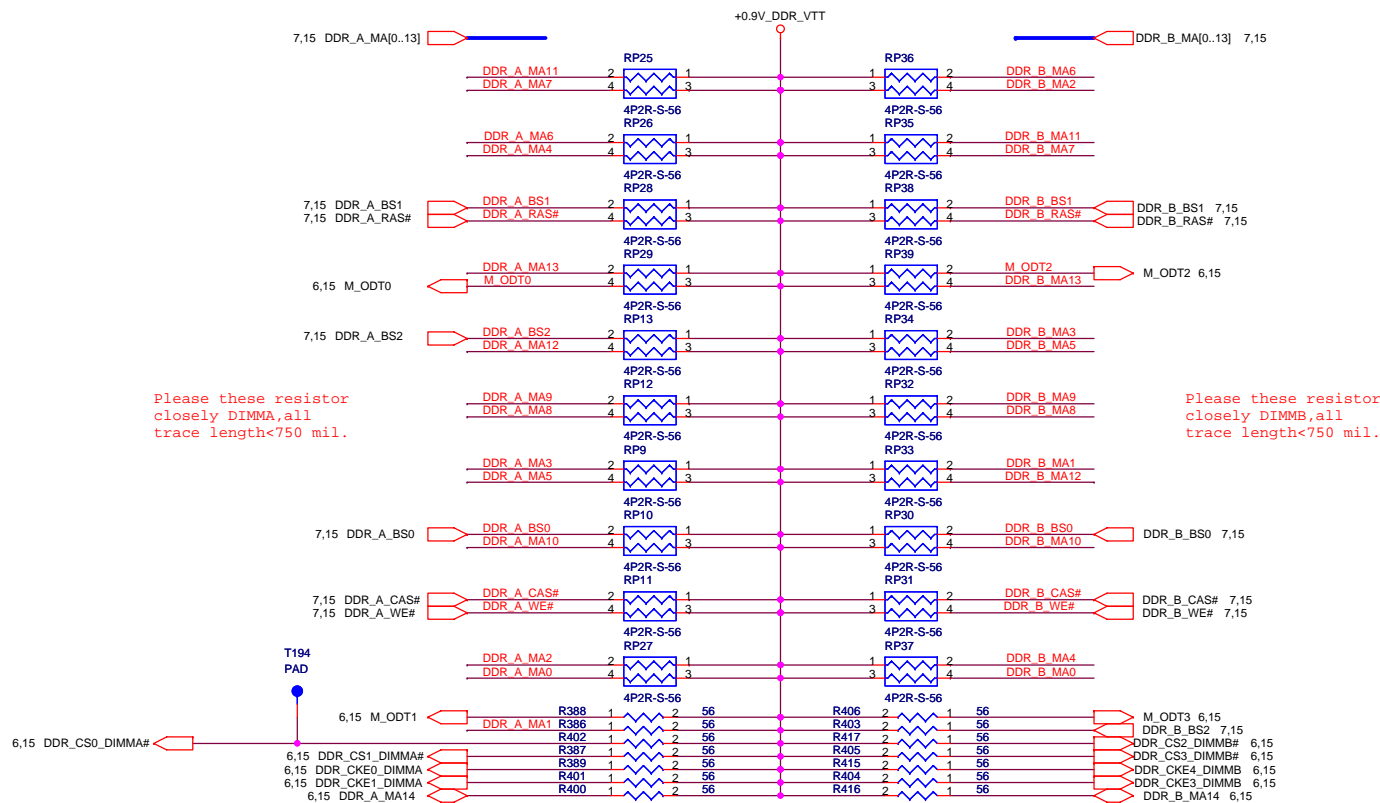
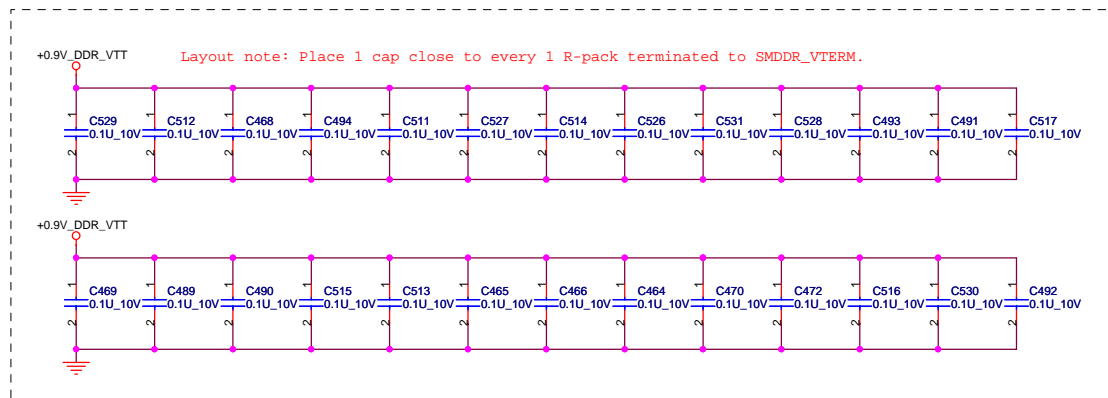
Size: Document Number GM3 Rev 2B

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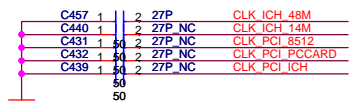


SLAVE

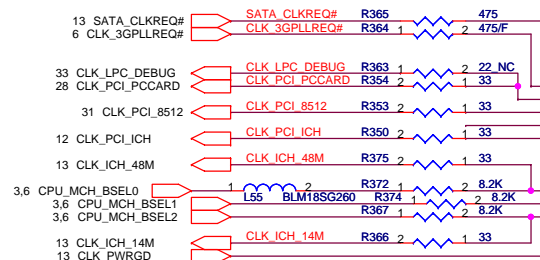




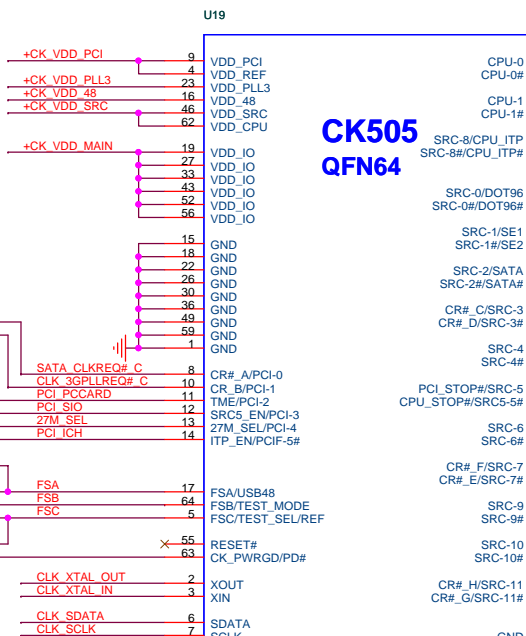
Add capacitor pads for improving WWAN.



14.318MHz



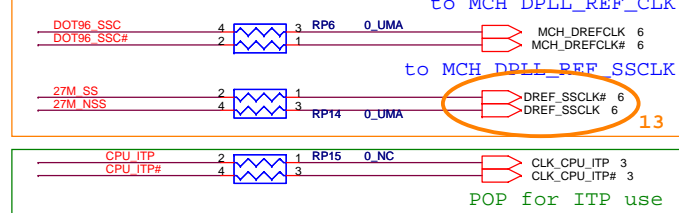
CLK_LPC_DEBUG FOR DEBUG
NEED POP RESISTOR



CK505
QFN64

SLG8SP513V

POP RESISTOR FOR UMA



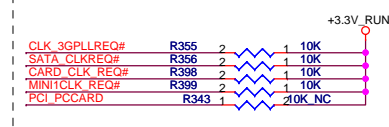
to MCH DPLL_REF_CLK

to MCH DPLL_REF_SSCLK

POP for ITP use

to ATI VGA

Silego need pull up
but other?

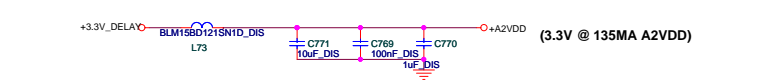
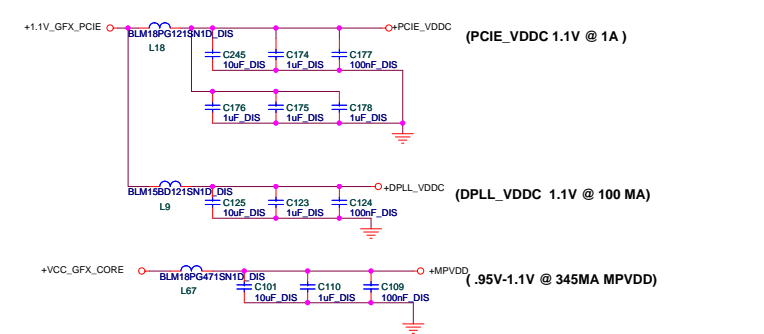
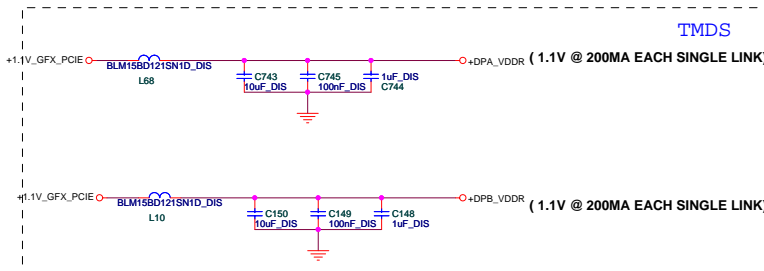
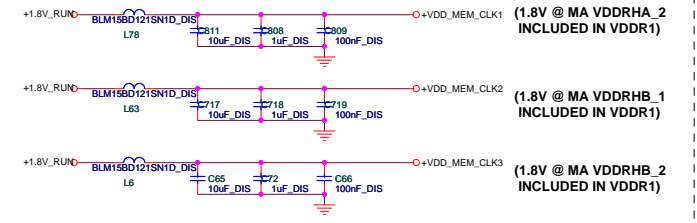
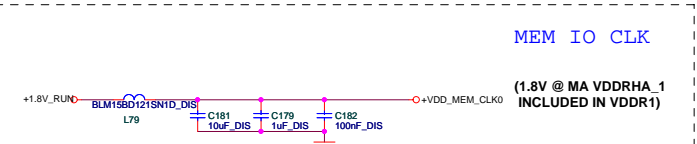
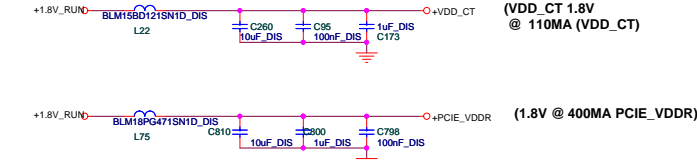
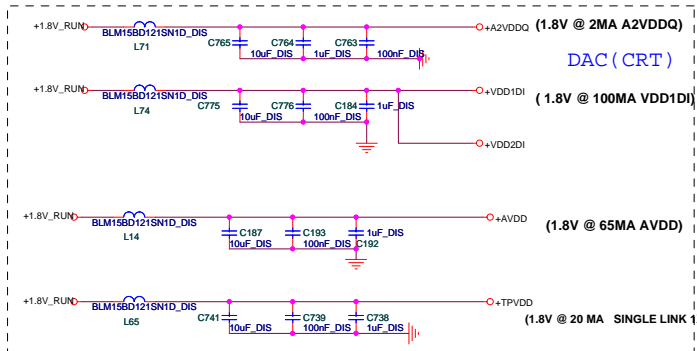
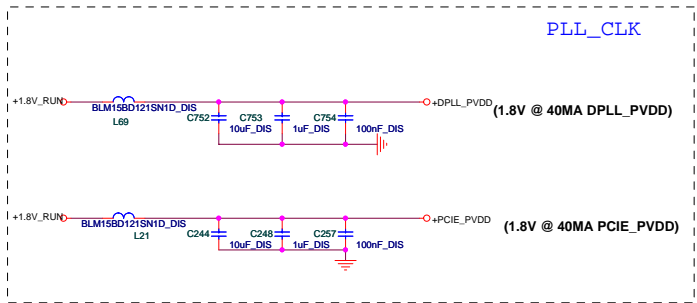
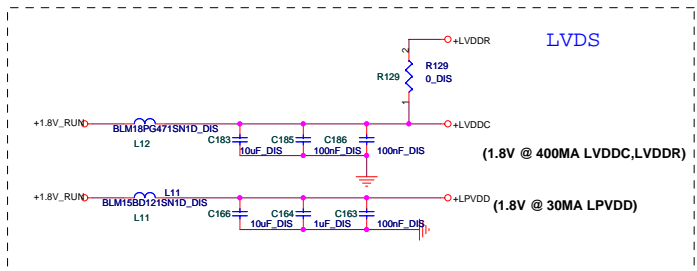


| FSC | FSB | FSA | CPU | SRC | PCI |
|-----|-----|-----|------|-----|-----|
| 1 | 0 | 1 | 100 | 100 | 33 |
| 0 | 0 | 1 | 133 | 100 | 33 |
| 0 | 1 | 1 | 166 | 100 | 33 |
| 0 | 0 | 0 | 266 | 100 | 33 |
| 1 | 0 | 0 | 333 | 100 | 33 |
| 1 | 1 | 0 | 400 | 100 | 33 |
| 1 | 1 | 1 | RSVD | 100 | 33 |

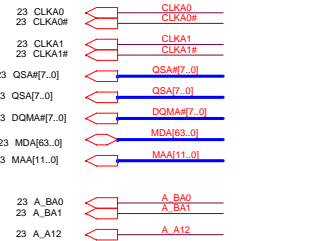
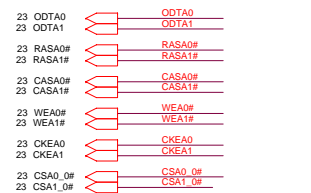
27M_SEL

| 27M_SEL (PIN13) | PIN20 | PIN21 | PIN24 | PIN25 |
|---------------------|--------|--------|-----------|-----------|
| 0=UMA | DOT96T | DOT96C | 96/100M_T | 96/100M_C |
| 1 = Disc. GRFX down | SRCT0 | SRCC0 | 27Mout | 27MSSout |

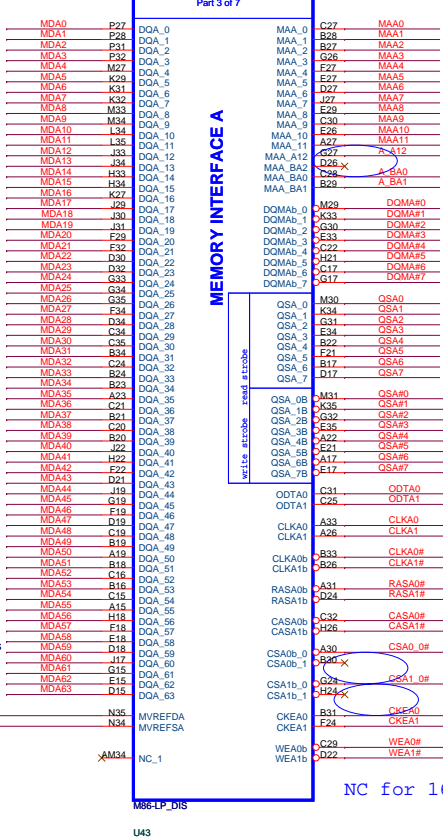
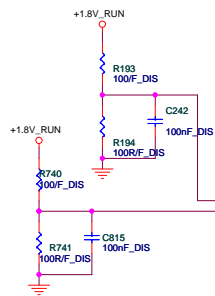
QUANTA
COMPUTER



PLACE ALL DECOUPLING AS CLOSE TO ASIC AS POSSIBLE

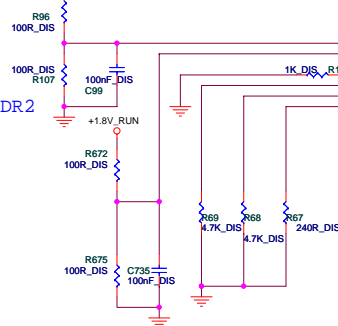


PLACE MVREF DIVIDERS
AND CAPS CLOSE TO ASIC



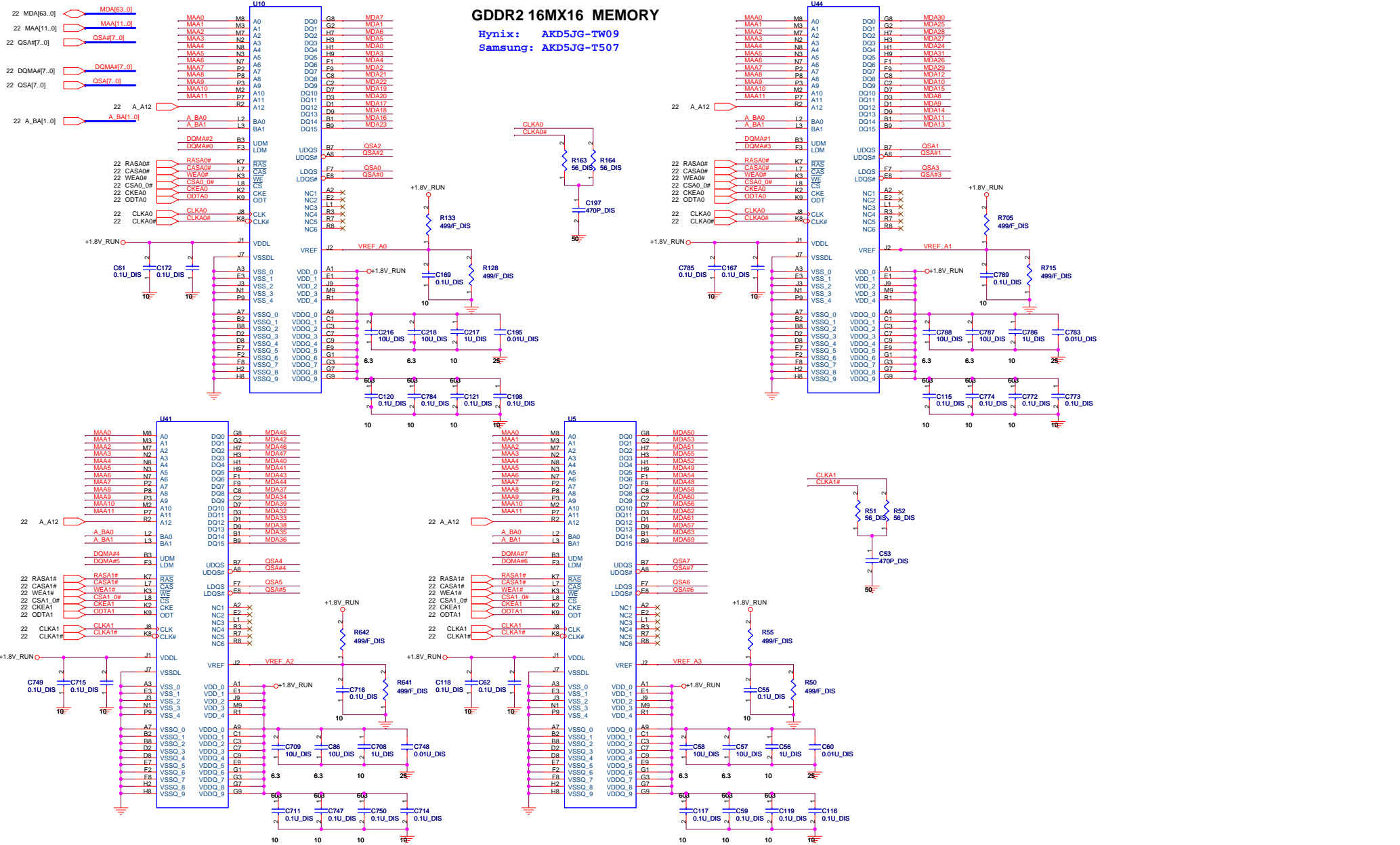
NC for 16M x16 DDR2

PLACE MVREF DIVIDERS
AND CAPS CLOSE TO ASIC



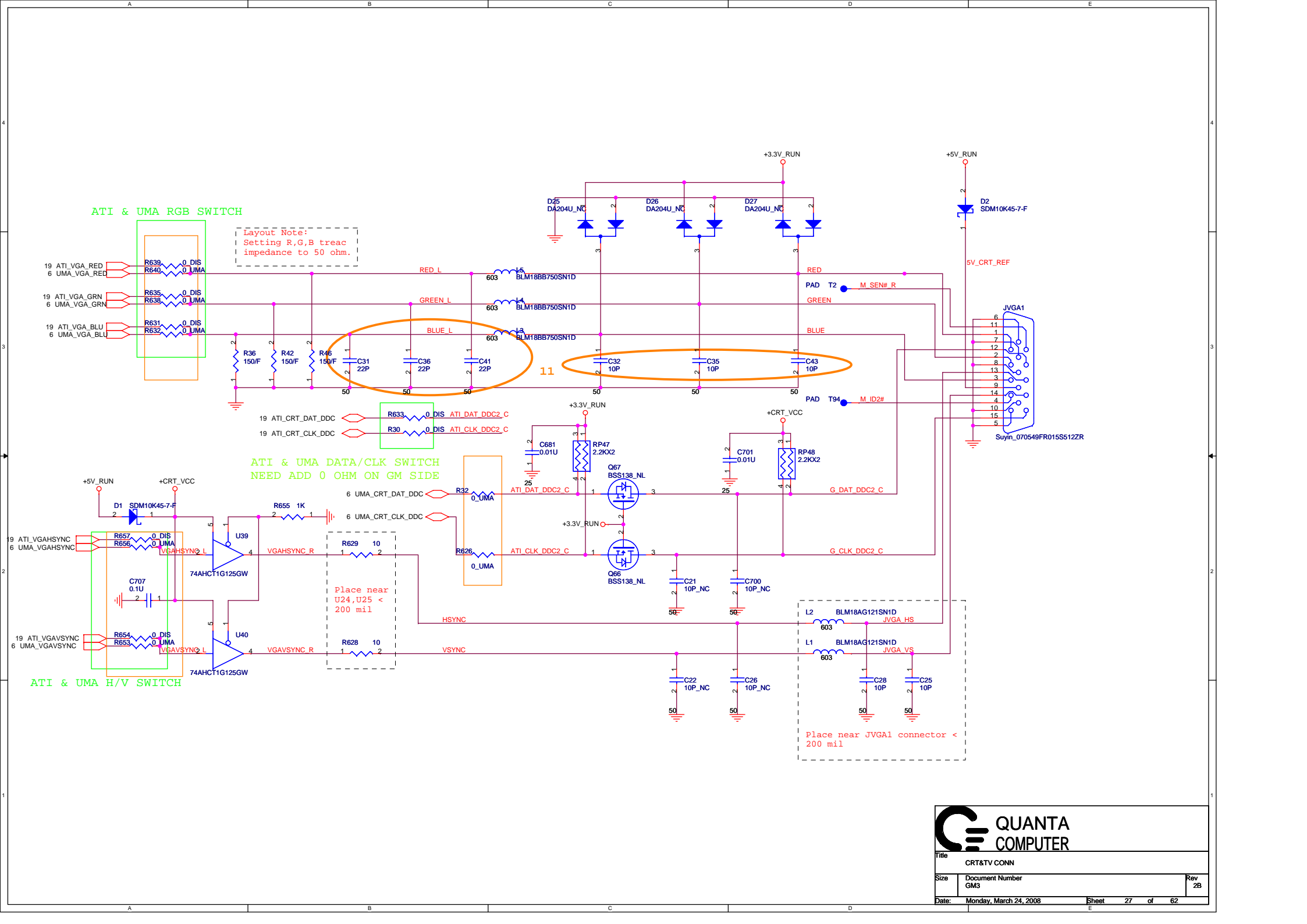
GDDR2 16MX16 MEMORY

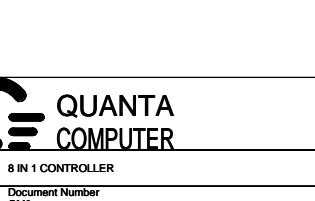
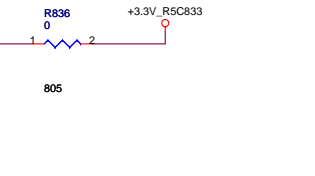
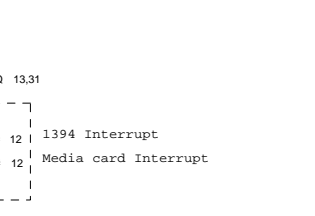
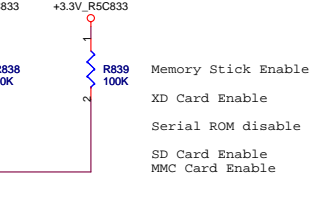
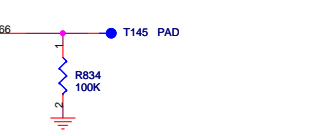
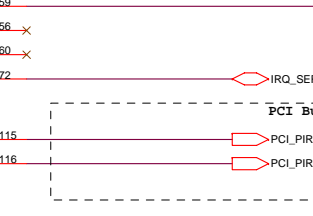
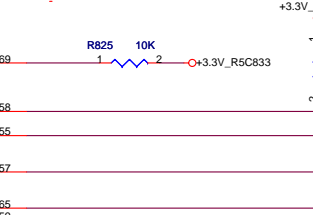
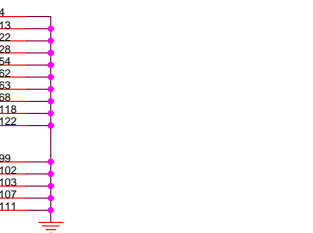
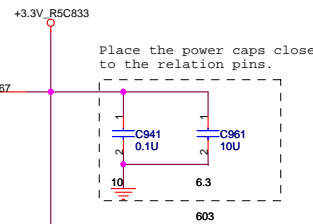
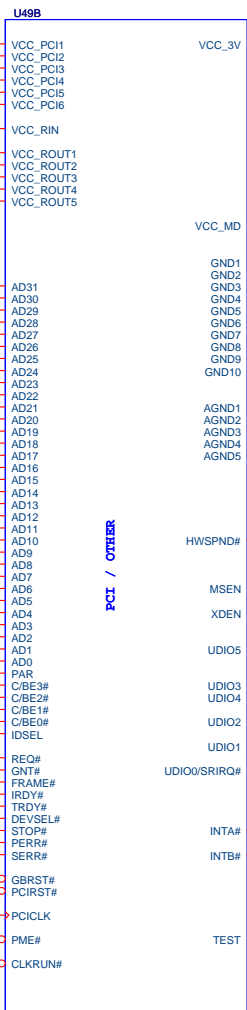
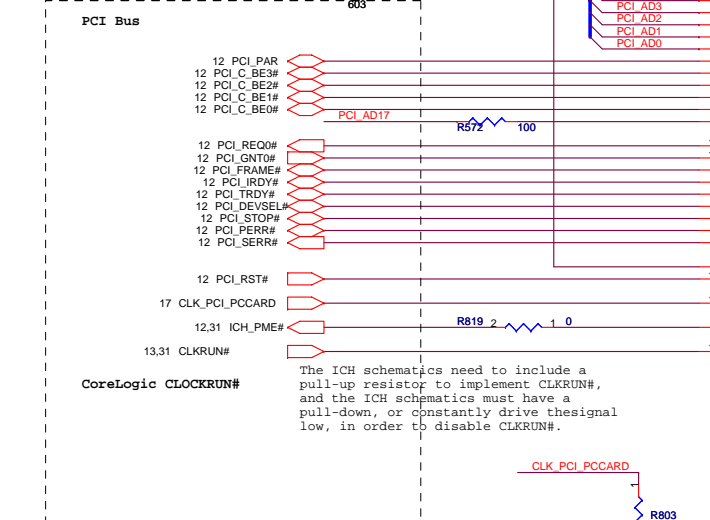
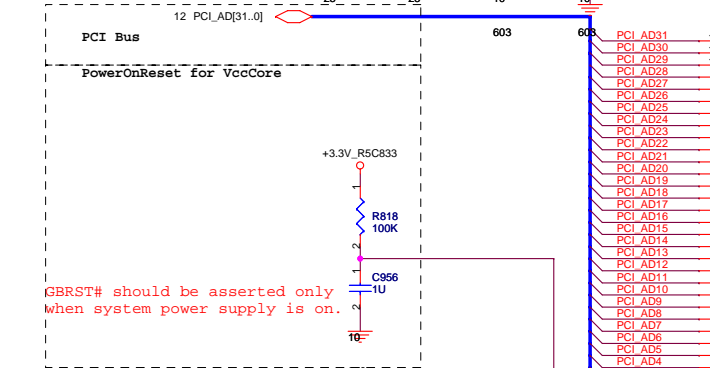
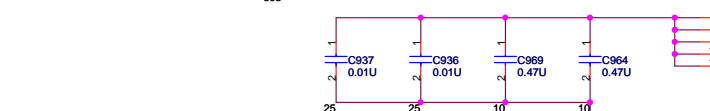
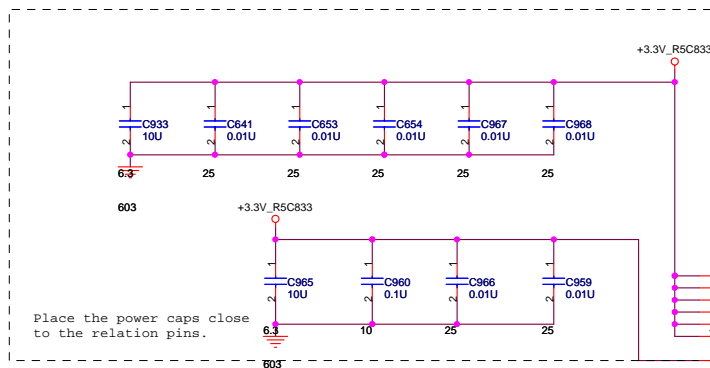
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Samsung: AKD5JG-T507

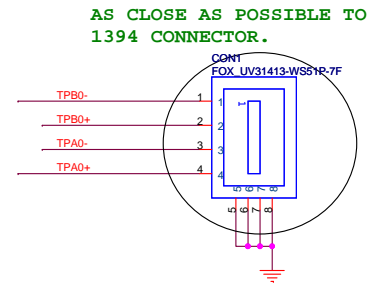
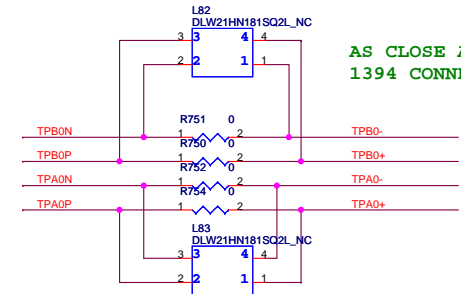
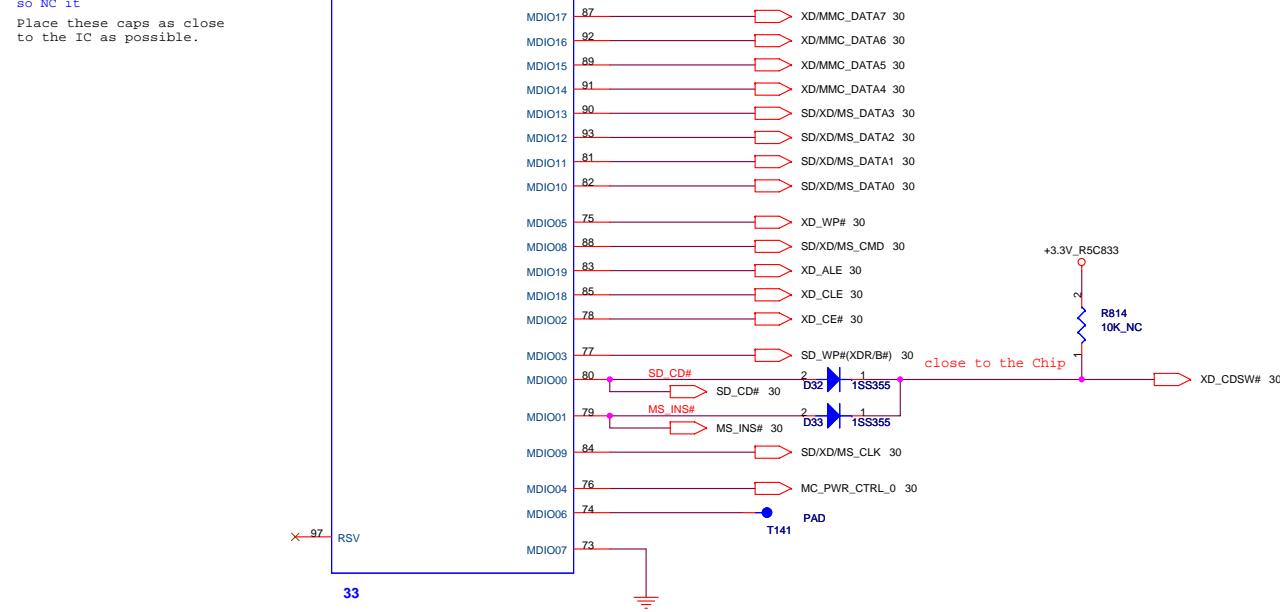
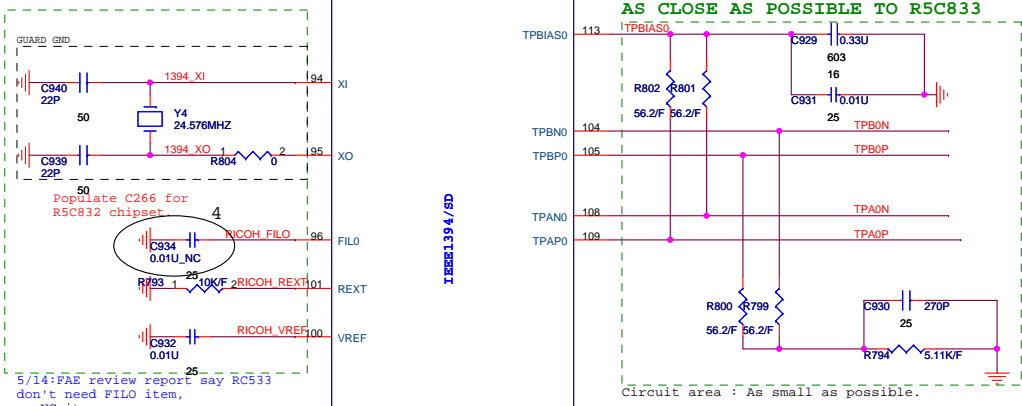
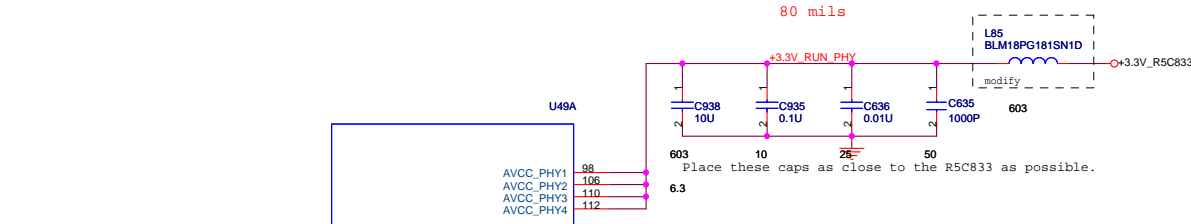


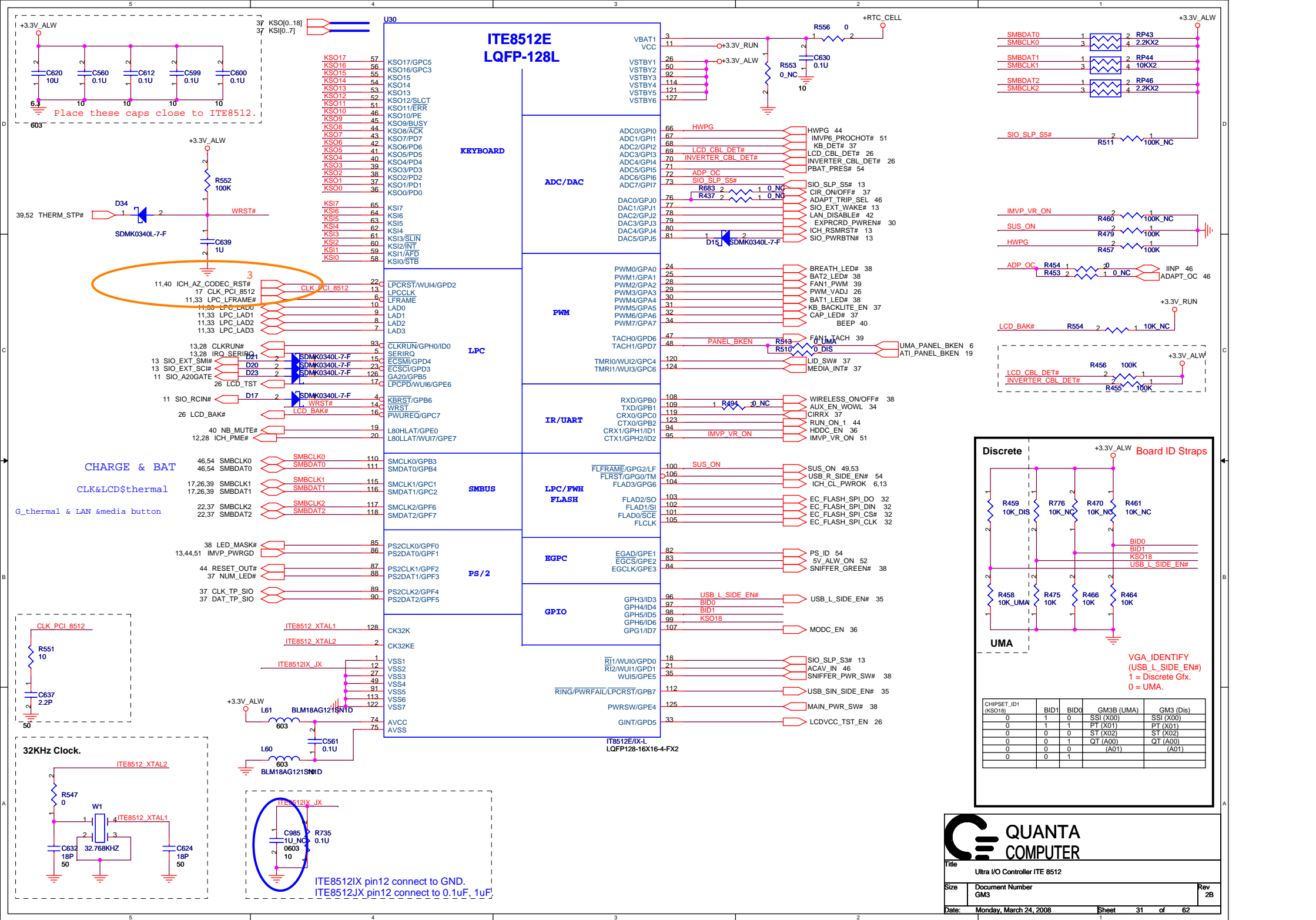
Hynix: AKD5JG-TW09
Samsung: AKD5JG-T507



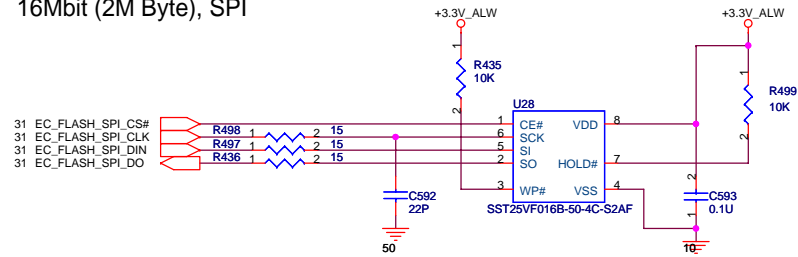




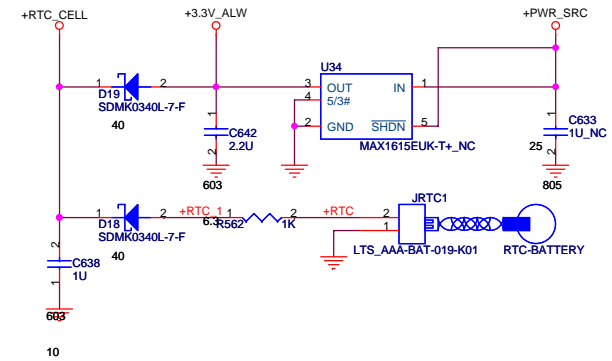




16Mbit (2M Byte), SPI

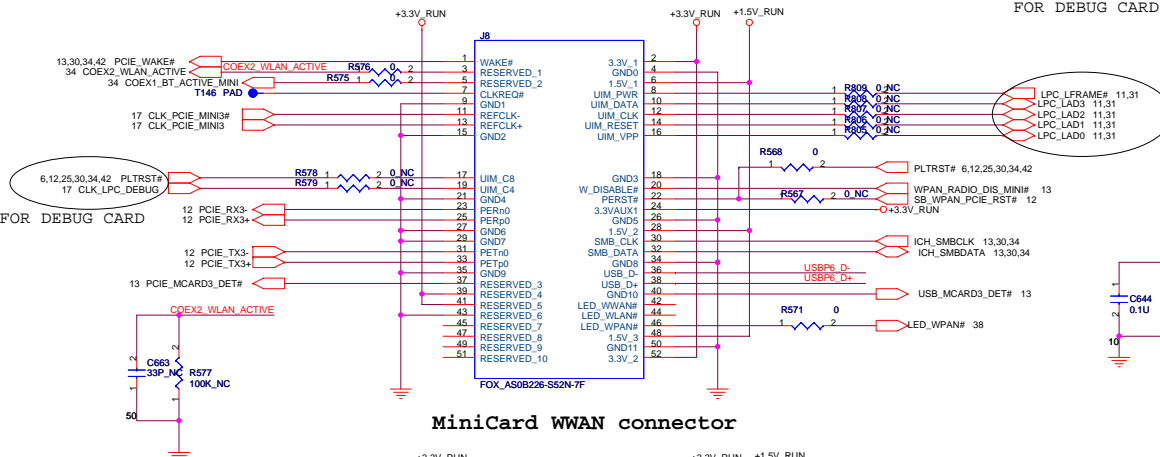


RTC BATTERY

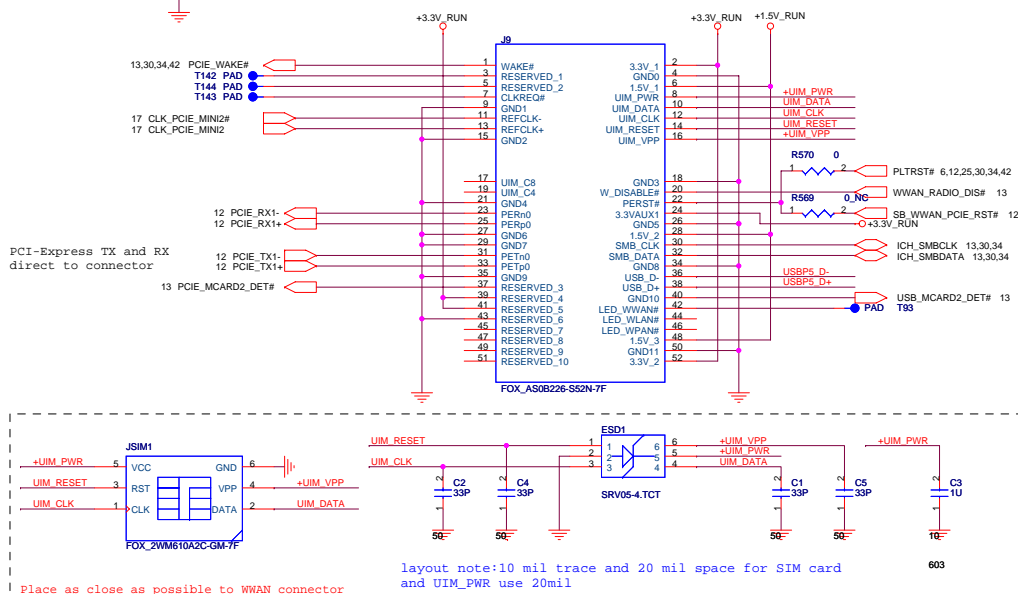


MiniCard Robson, UWB connector

FOR DEBUG CARD

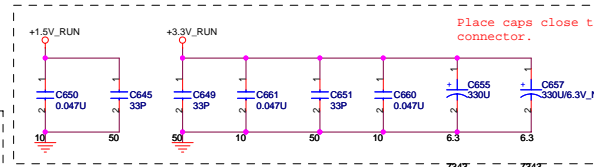
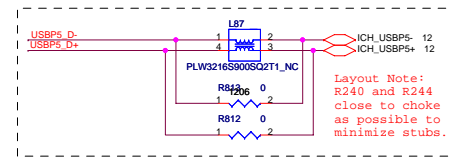
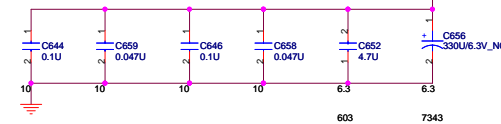
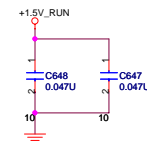
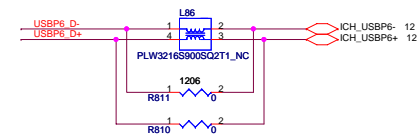


MiniCard WWAN connector

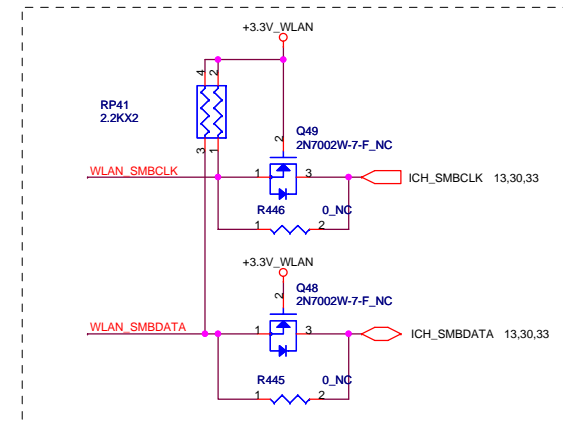
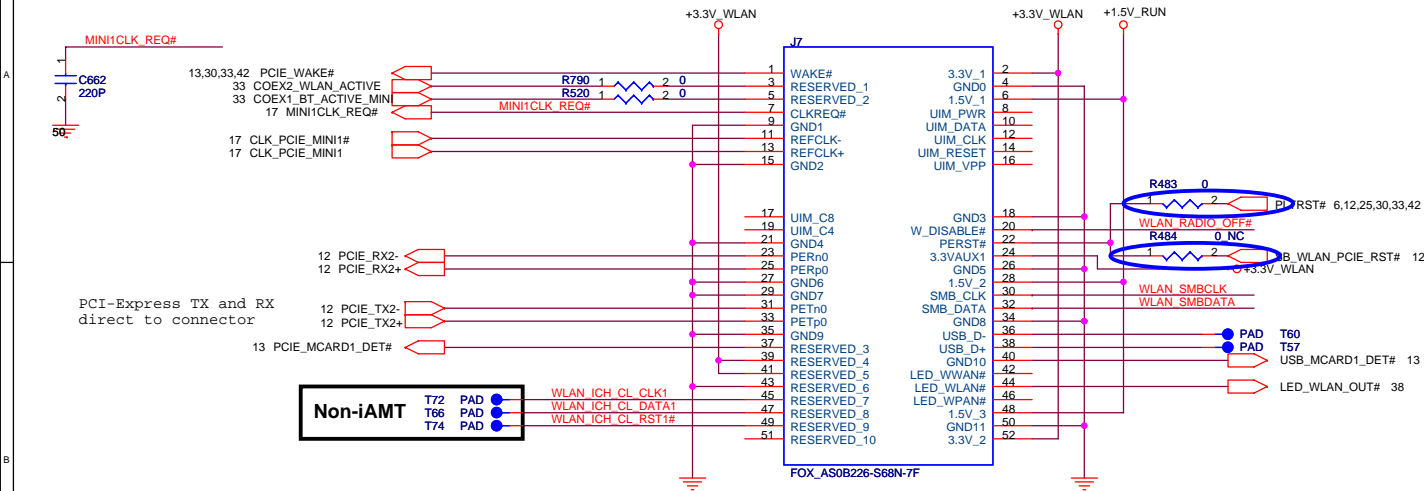


layout note:10 mil trace and 20 mil space for SIM card and UIM_PWR use 20mil

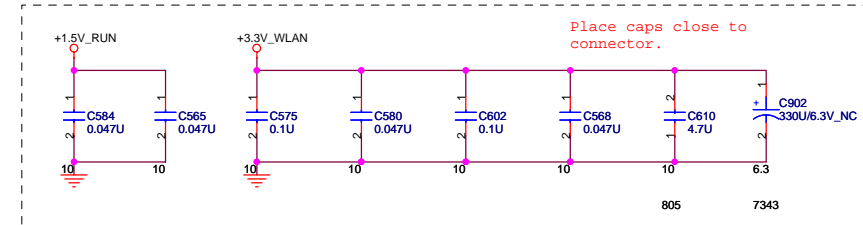
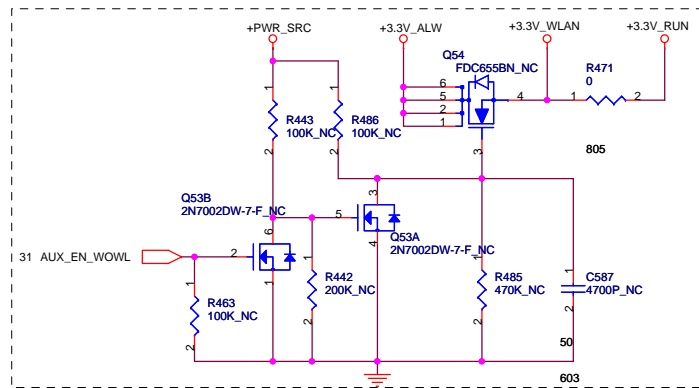
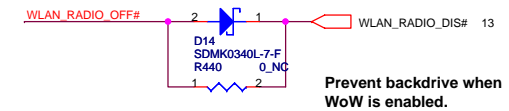
Place as close as possible to WWAN connector



MiniCard WLAN connector



Suport for WoW



Title

| | |
|------|------|
| File | WLAN |
|------|------|

Size

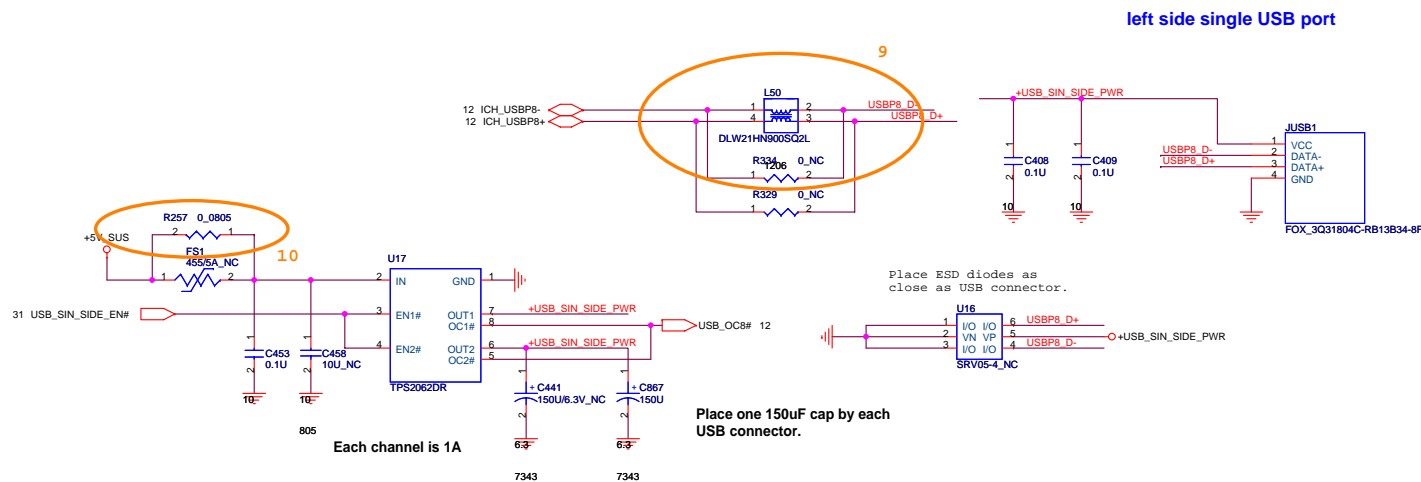
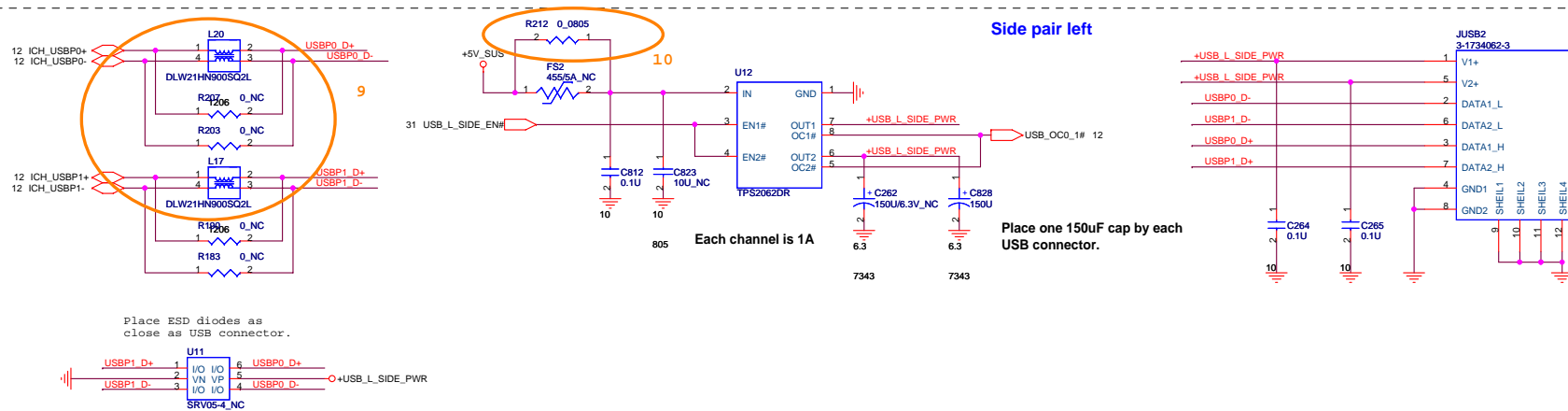
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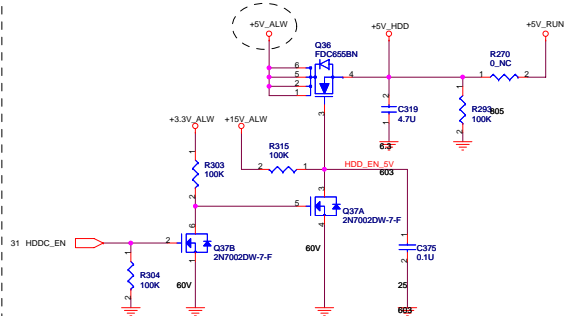
Date: Monday, March 24, 2008

Sheet 34 of 62

| | | |
|----|----|----|
| 34 | 01 | 02 |
| 8 | | |

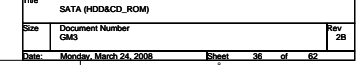
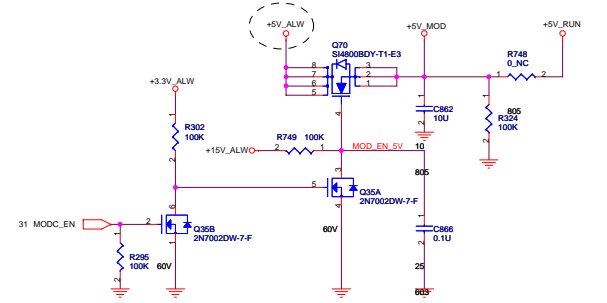


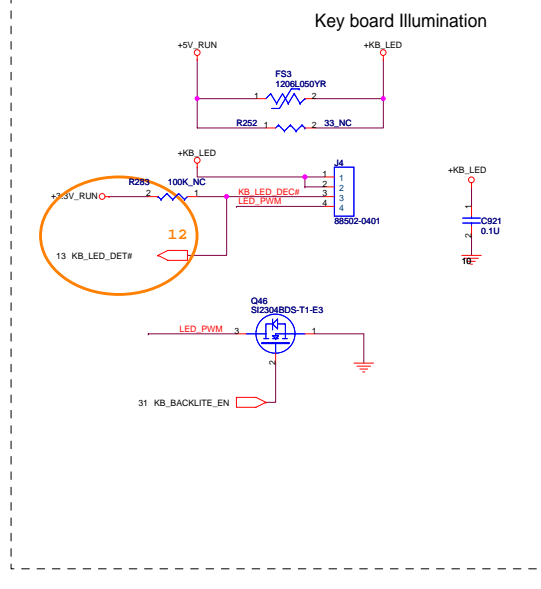
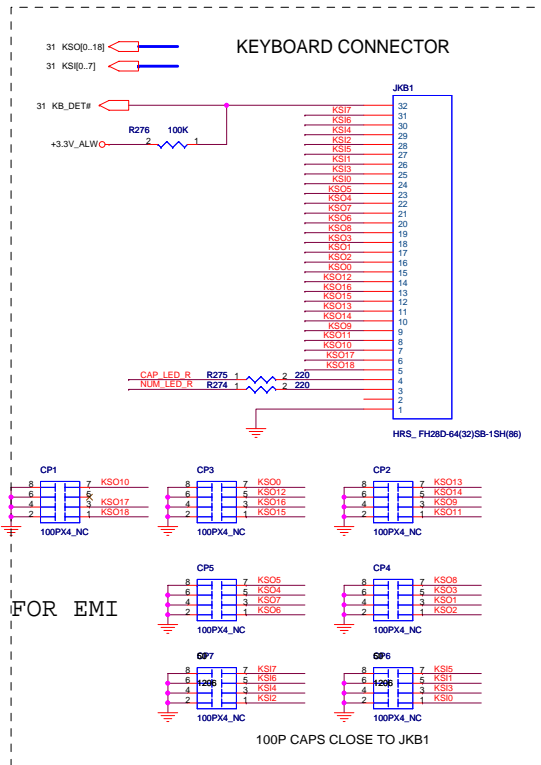
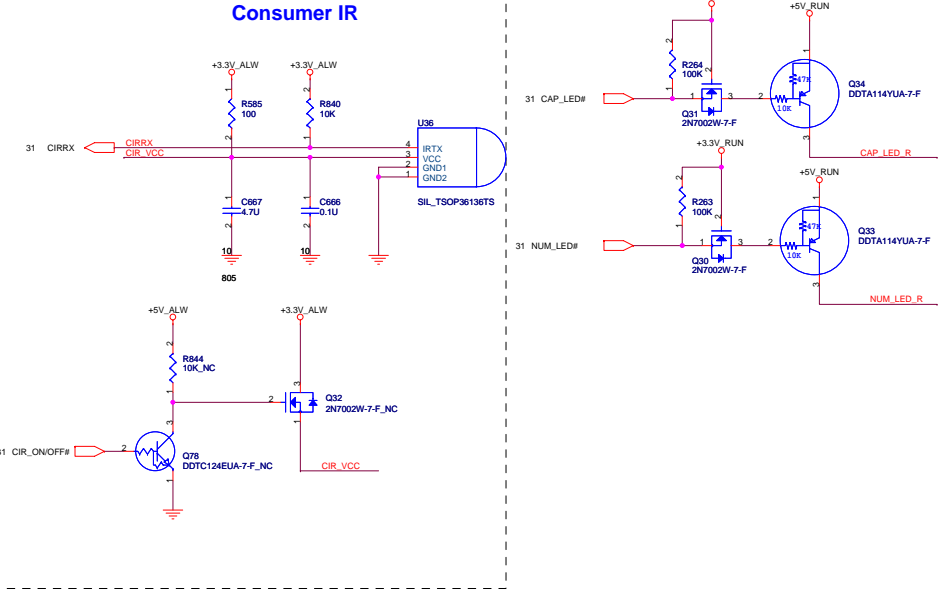
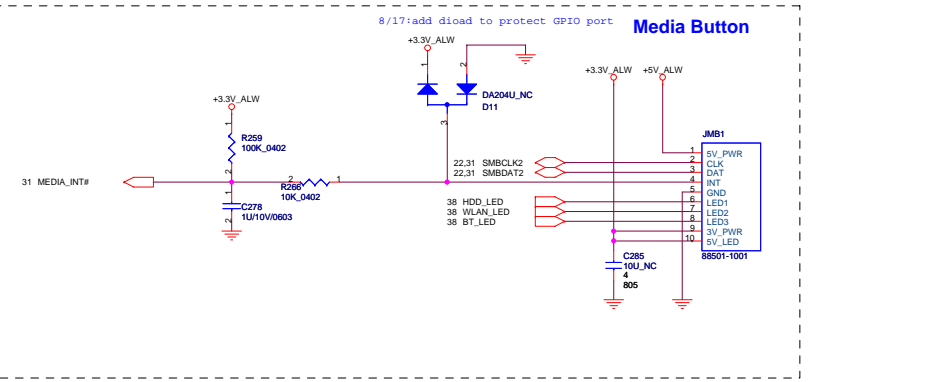
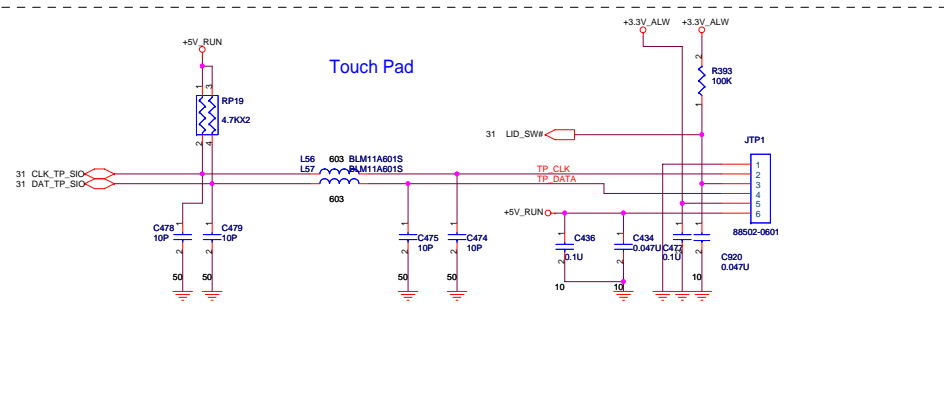
Second HDD



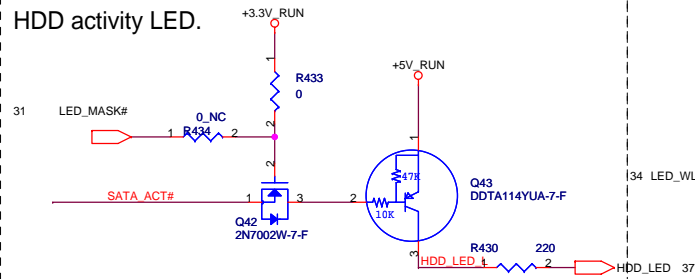
Place caps close to SATA1 connector.

The diagram shows a power filtering circuit for the SATA1 connector. A +5V_HDD input is connected to a series of capacitors: C904 (10u/10V/0805), C909 (1u/10V/0603), C908 (0.1u/16V), C905 (0.1u/16V), and C906 (1000p/50V). The capacitors are connected in series between the +5V_HDD line and the SATA1 connector.

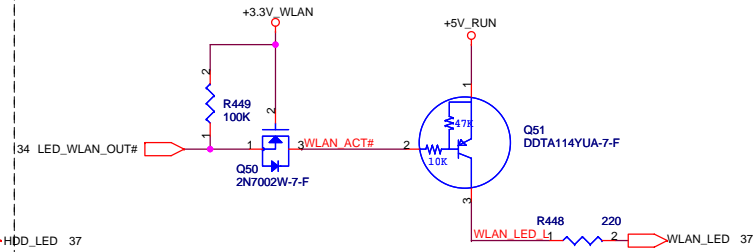




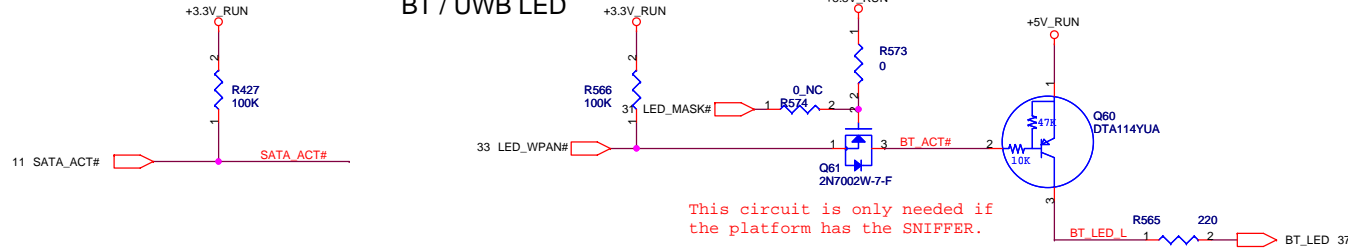
HDD activity LED.



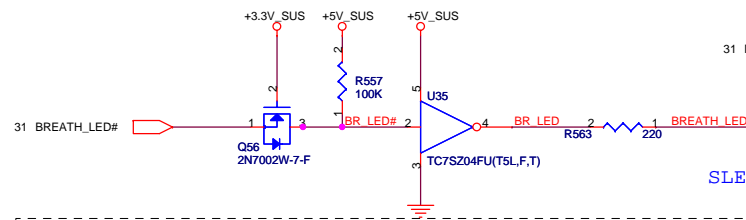
WLAN



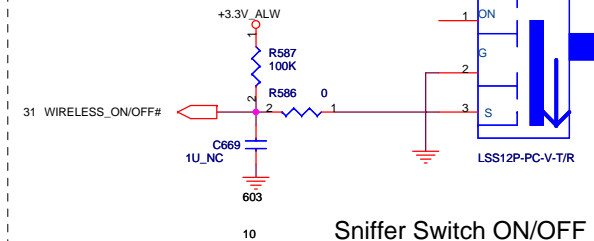
BT / UWB LED



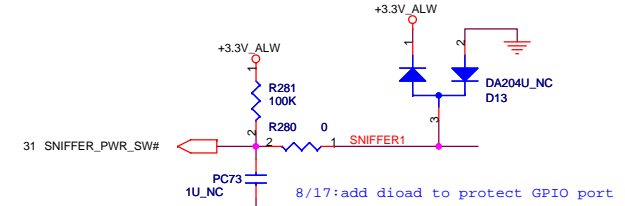
Power & Suspend.



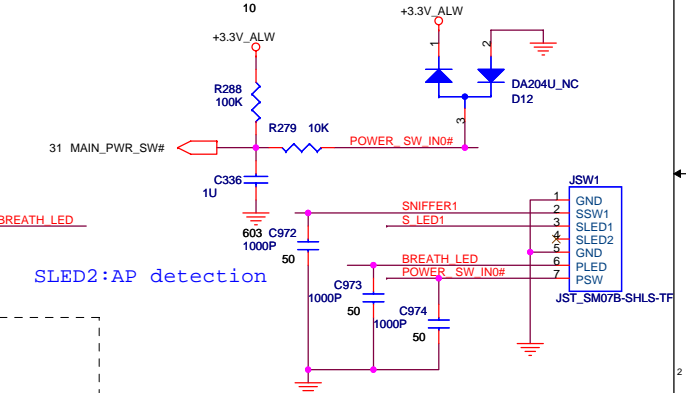
Sniffer Switch



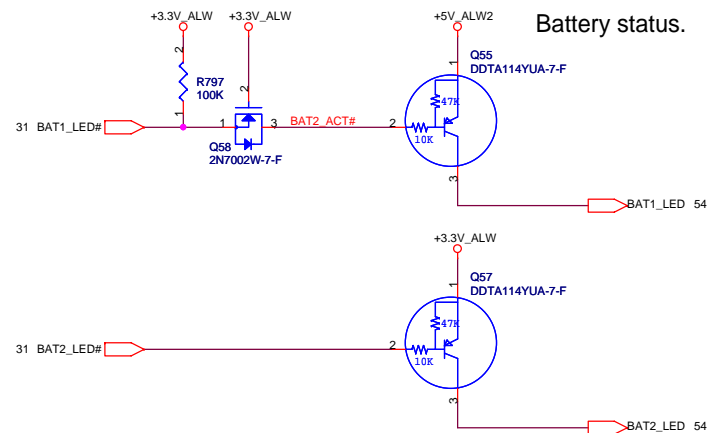
Sniffer Switch ON/OFF



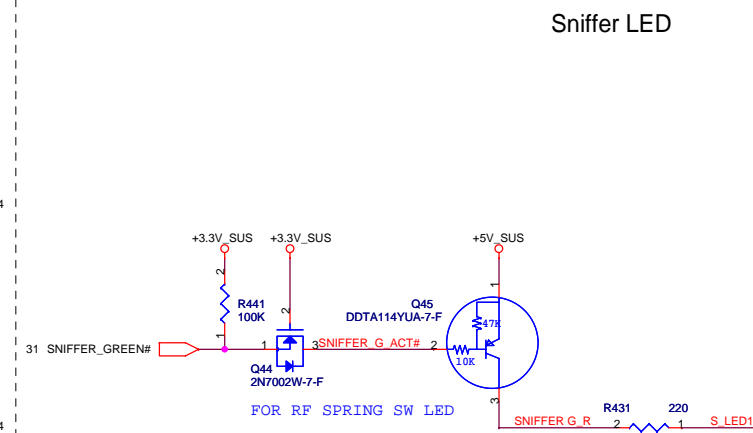
Power Switch



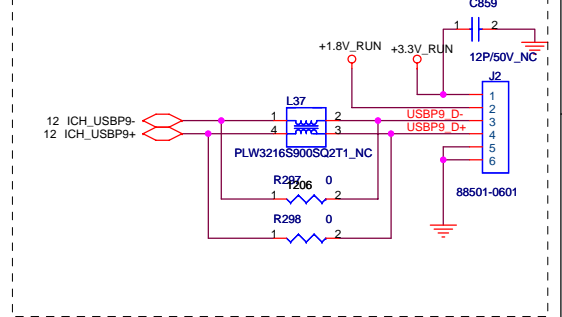
Battery status.



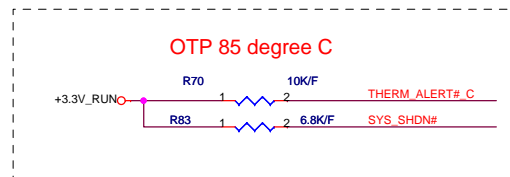
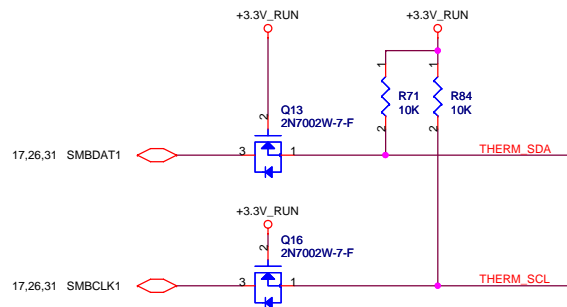
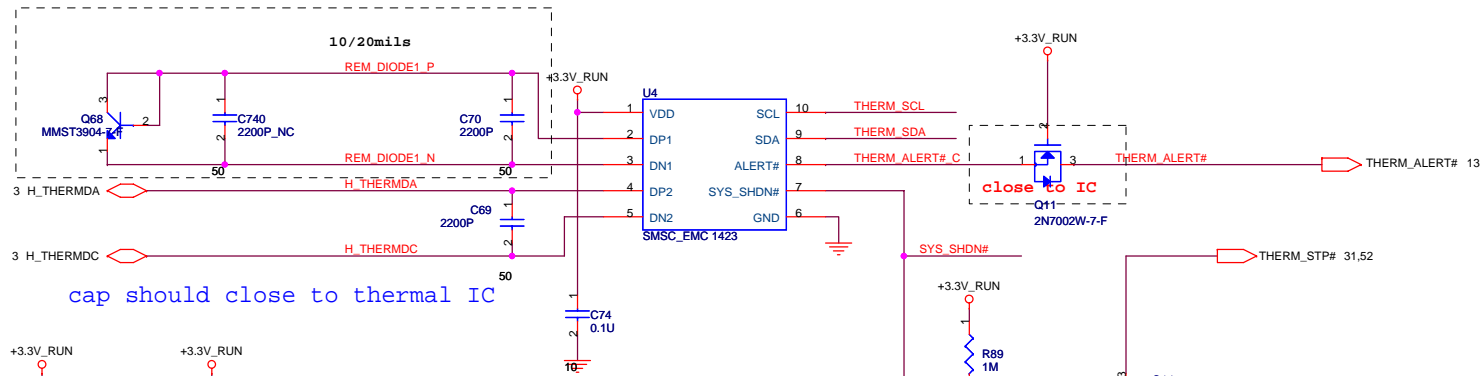
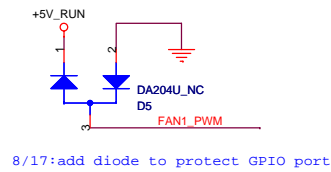
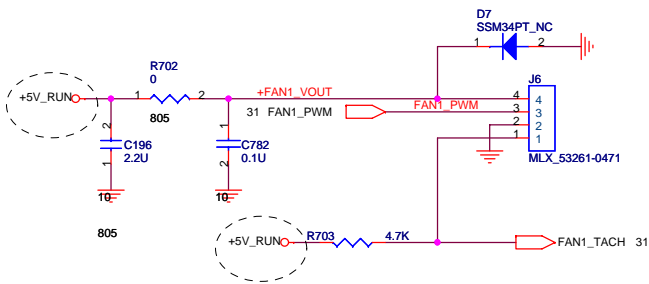
Sniffer LED



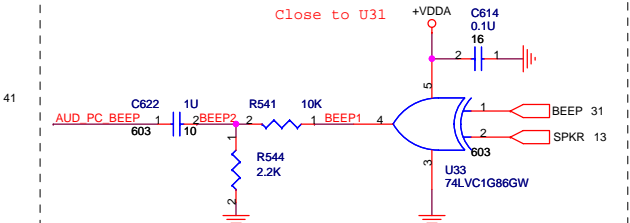
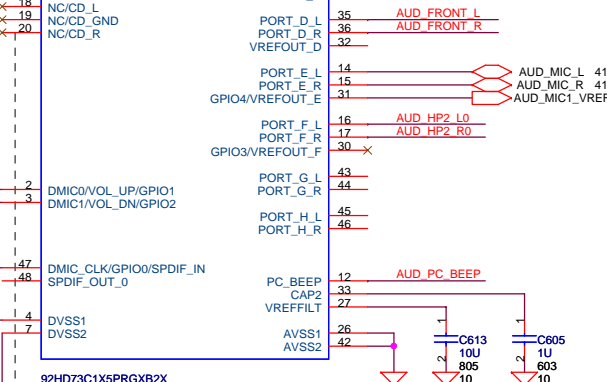
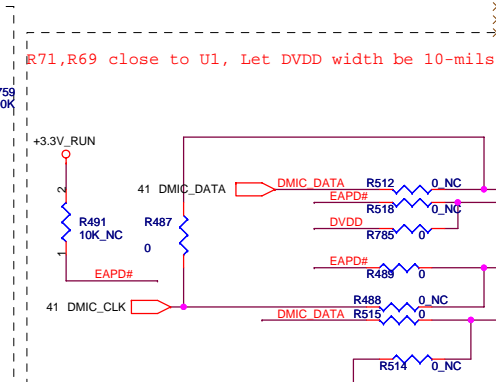
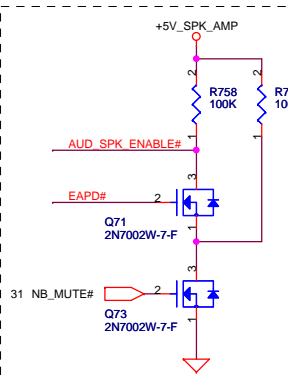
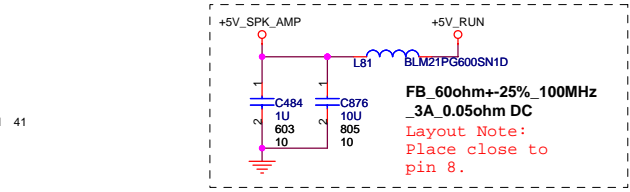
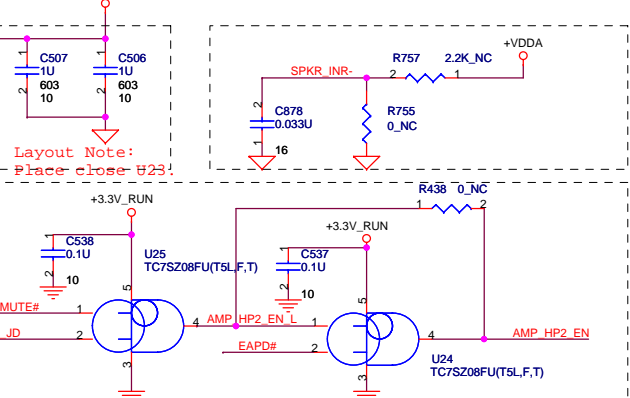
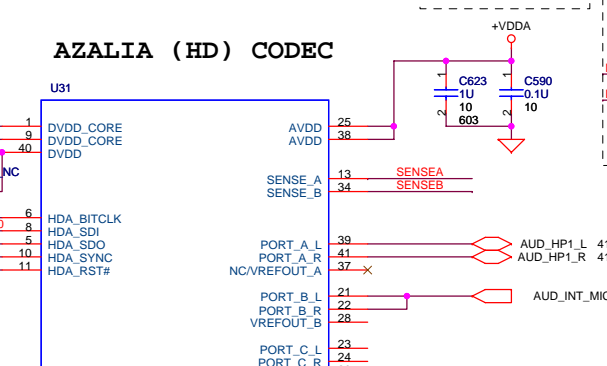
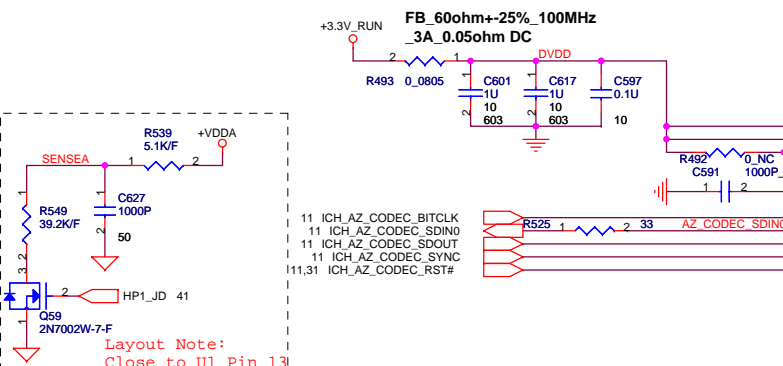
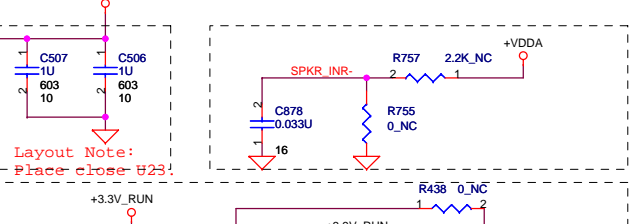
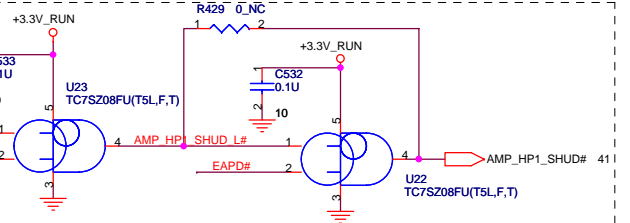
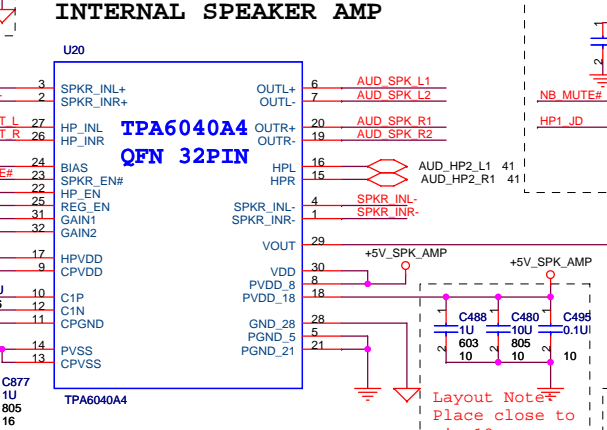
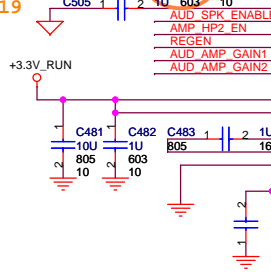
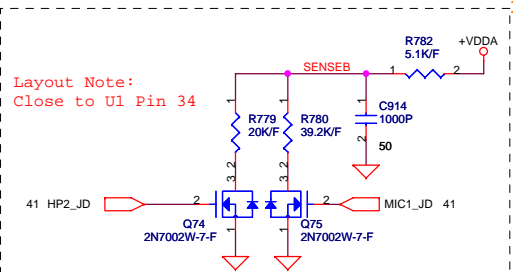
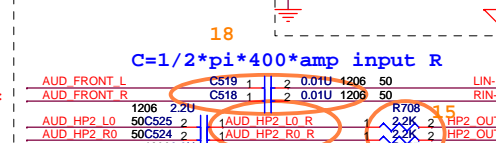
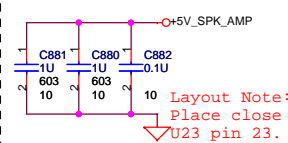
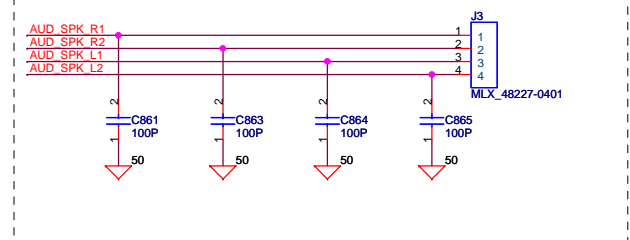
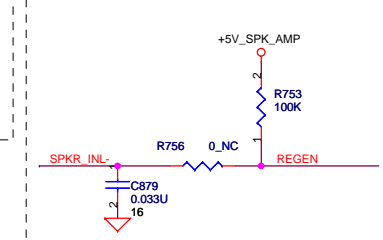
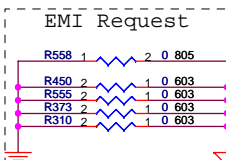
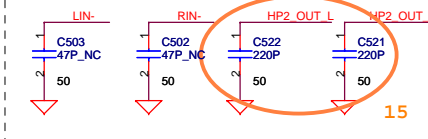
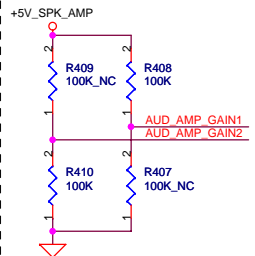
Biometric



| | | | |
|-------|------------------------|-------|------------------------|
| Title | | | SWITCH, KEYBOARD & LED |
| Size | Document Number | Rev | |
| GM3 | | 2B | |
| Date: | Monday, March 24, 2008 | Sheet | 38 of 62 |



| GAIN1 | GAIN2 | GAIN |
|-------|-------|--------|
| 0 | 0 | 6dB |
| 0 | 1 | 10dB |
| 1 | 0 | 15.6dB |
| 1 | 1 | 21.6dB |



QUANTA COMPUTER

Title: Azelia CODEC

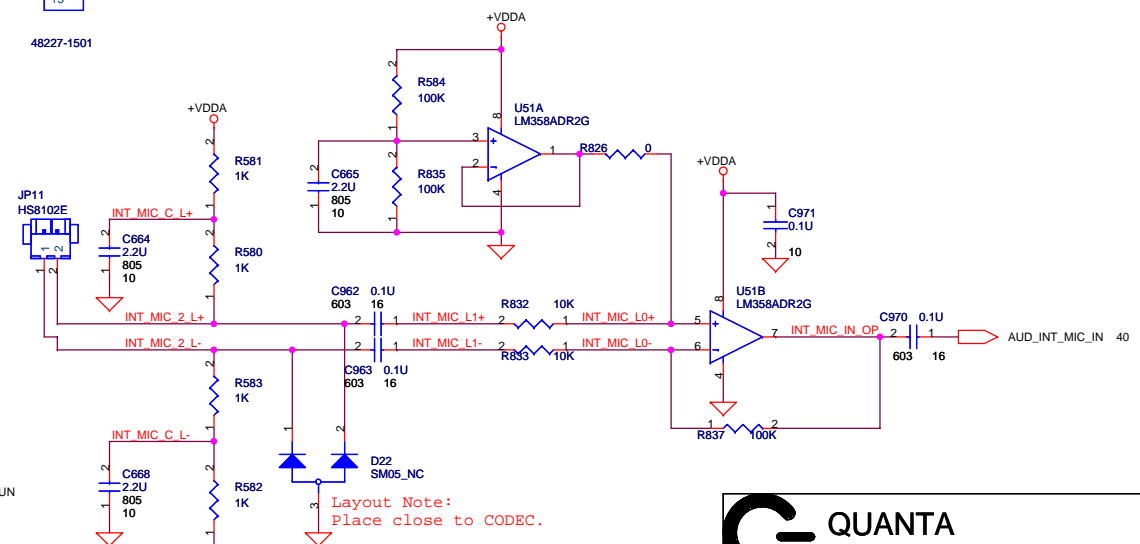
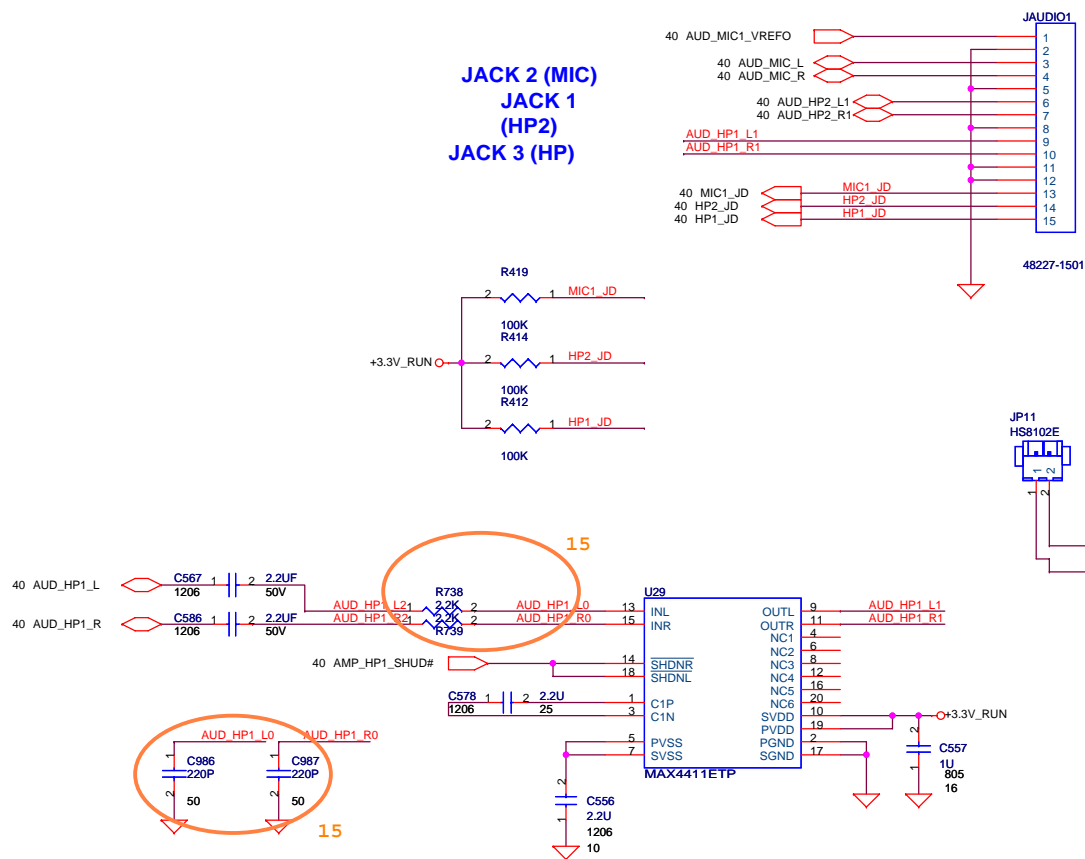
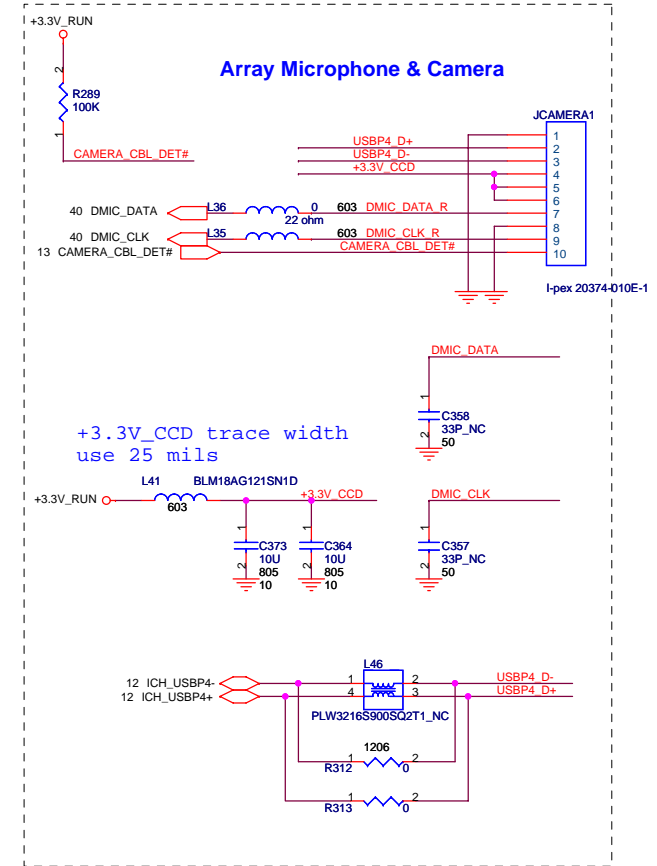
Size: GM3

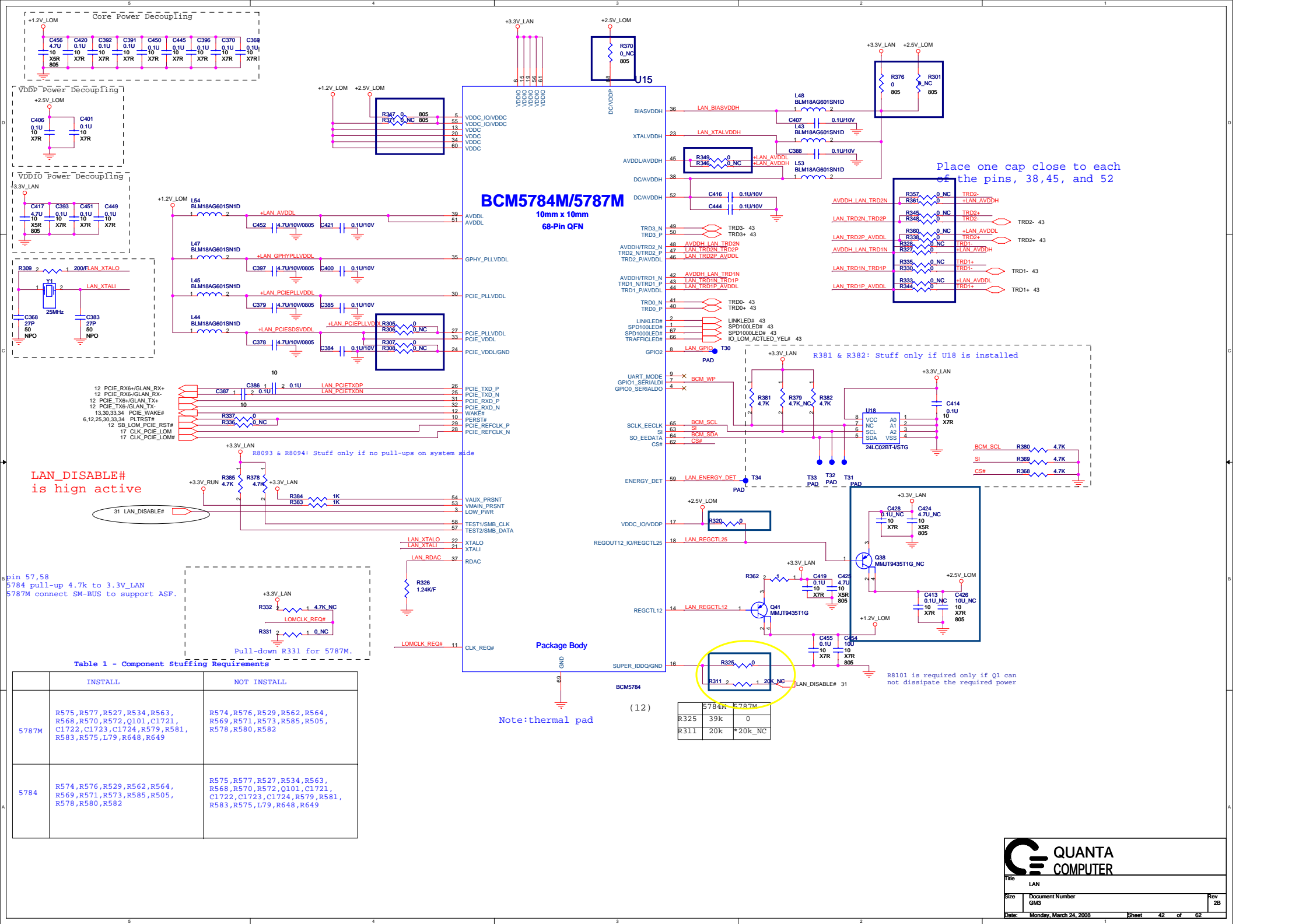
Date: Monday, March 24, 2008

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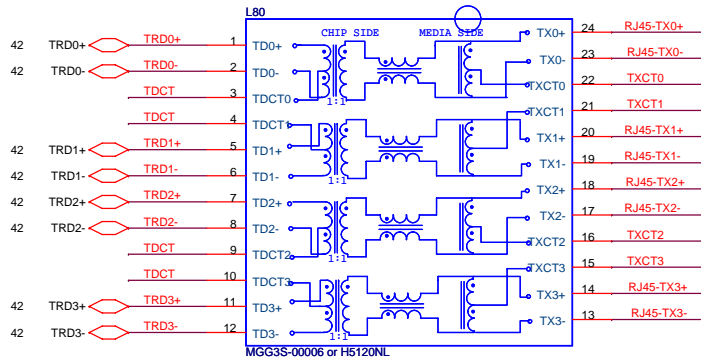
Rev: 2B

Headphone Jack
Stereo MIC Jack

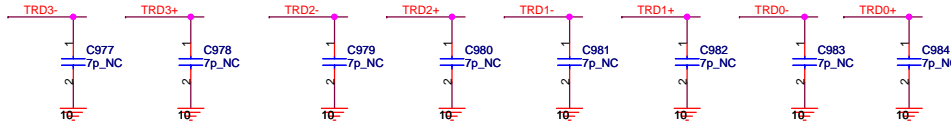




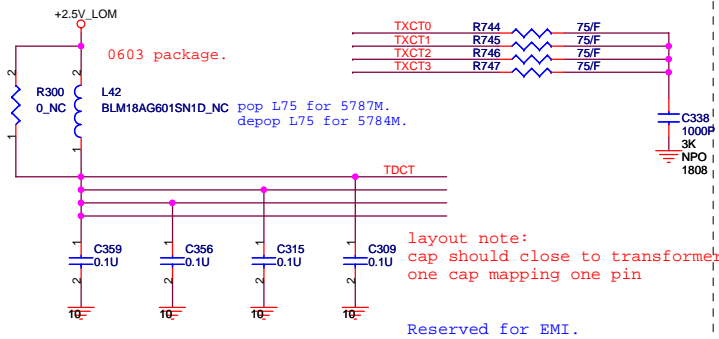
TRANSFORM



MGG3S-00006 or H5120NL

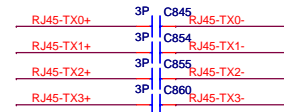


FOR EMI requirement and should close to L80



layout note:
cap should close to transformer
one cap mapping one pin

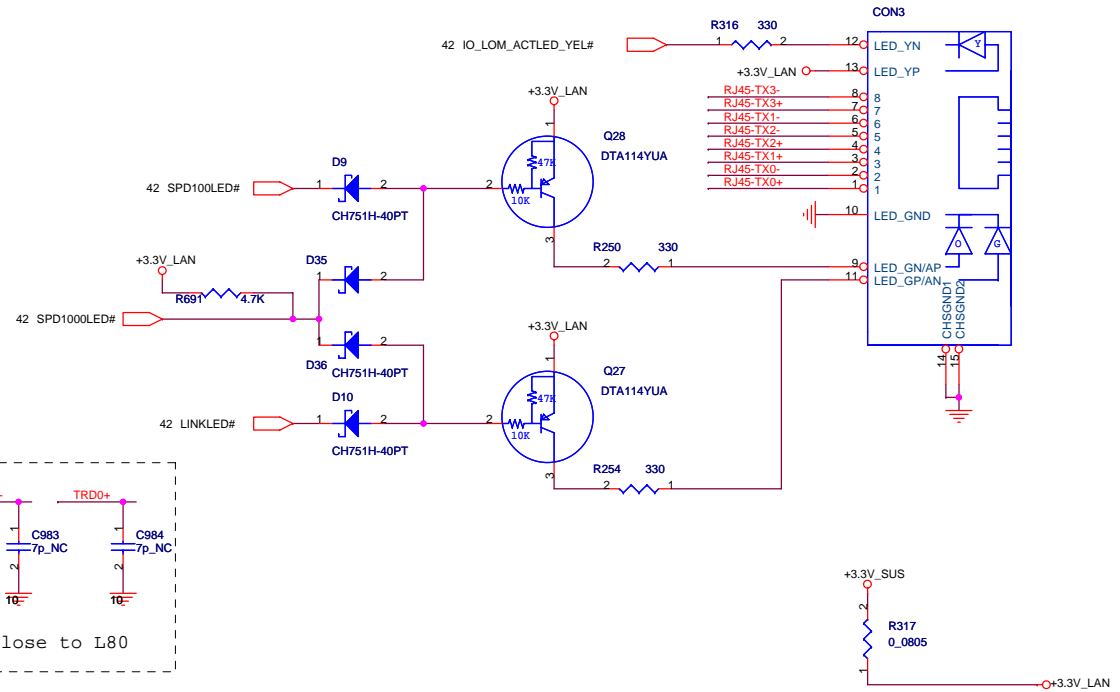
Reserved for EMI.

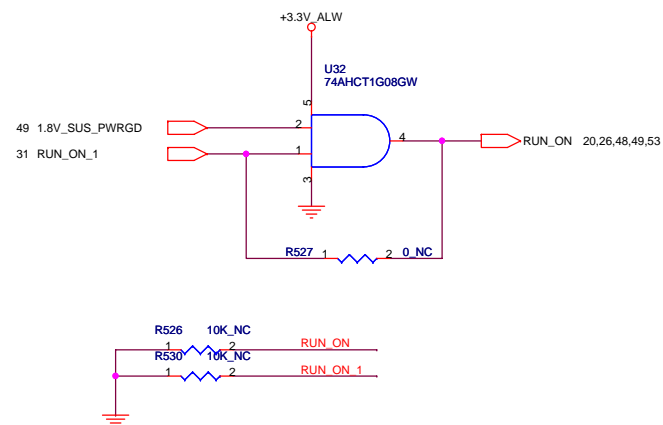
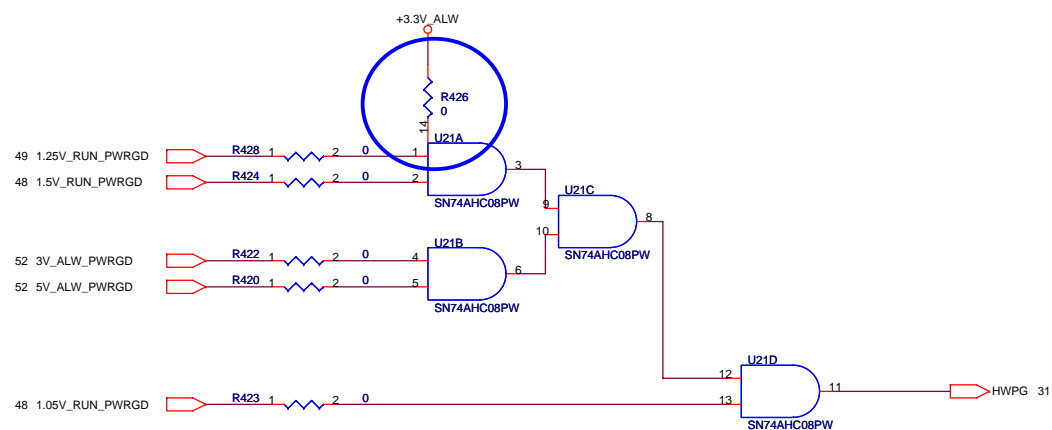
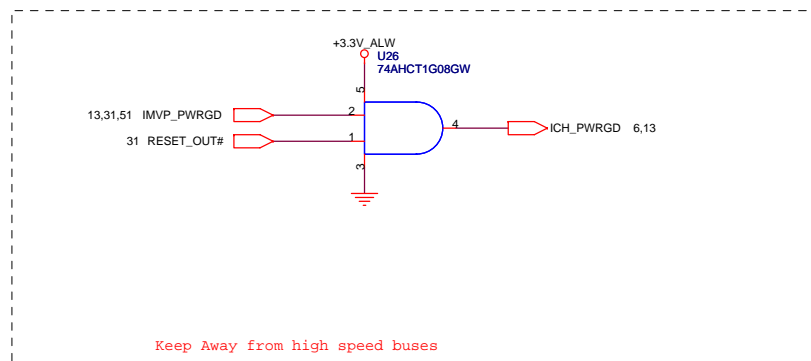


layout note:
cap should close to CONN

Reserved for EMI.

RJ-45 Connector







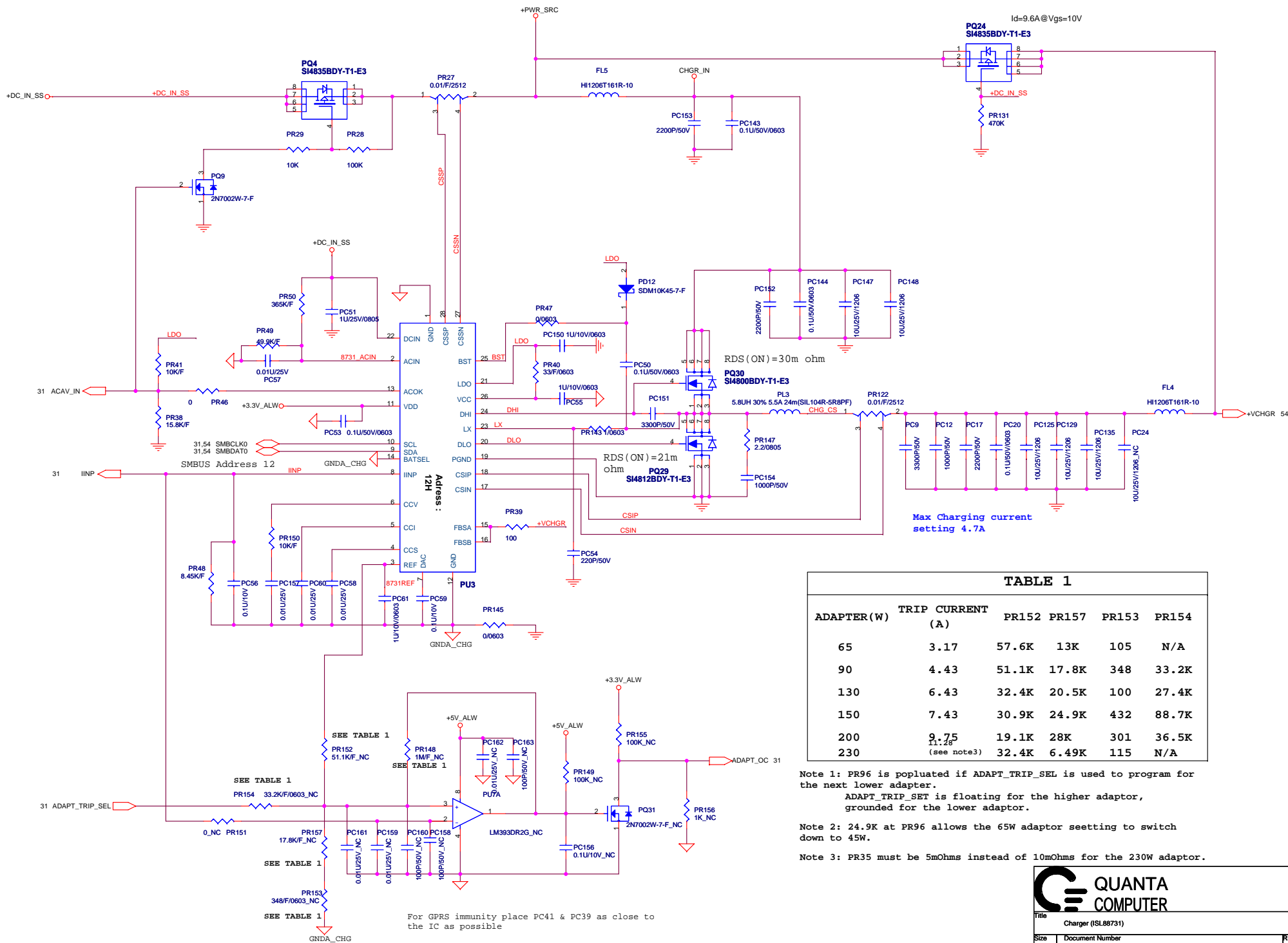


TABLE 1

| ADAPTER (W) | TRIP CURRENT (A) | PR152 | PR157 | PR153 | PR154 |
|-------------|------------------|-------|-------|-------|-------|
| 65 | 3.17 | 57.6K | 13K | 105 | N/A |
| 90 | 4.43 | 51.1K | 17.8K | 348 | 33.2K |
| 130 | 6.43 | 32.4K | 20.5K | 100 | 27.4K |
| 150 | 7.43 | 30.9K | 24.9K | 432 | 88.7K |
| 200 | 9.75 | 19.1K | 28K | 301 | 36.5K |
| 230 | (see note3) | 32.4K | 6.49K | 115 | N/A |

Note 1: PR96 is populated if ADAPT_TRIP_SEL is used to program for the next lower adaptor.

ADAPT_TRIP_SET is floating for the higher adaptor, grounded for the lower adaptor.

Note 2: 24.9K at PR96 allows the 65W adaptor setting to switch down to 45W.


Note 3: PR35 must be 5mOhms instead of 10mOhms for the 230W adaptor.

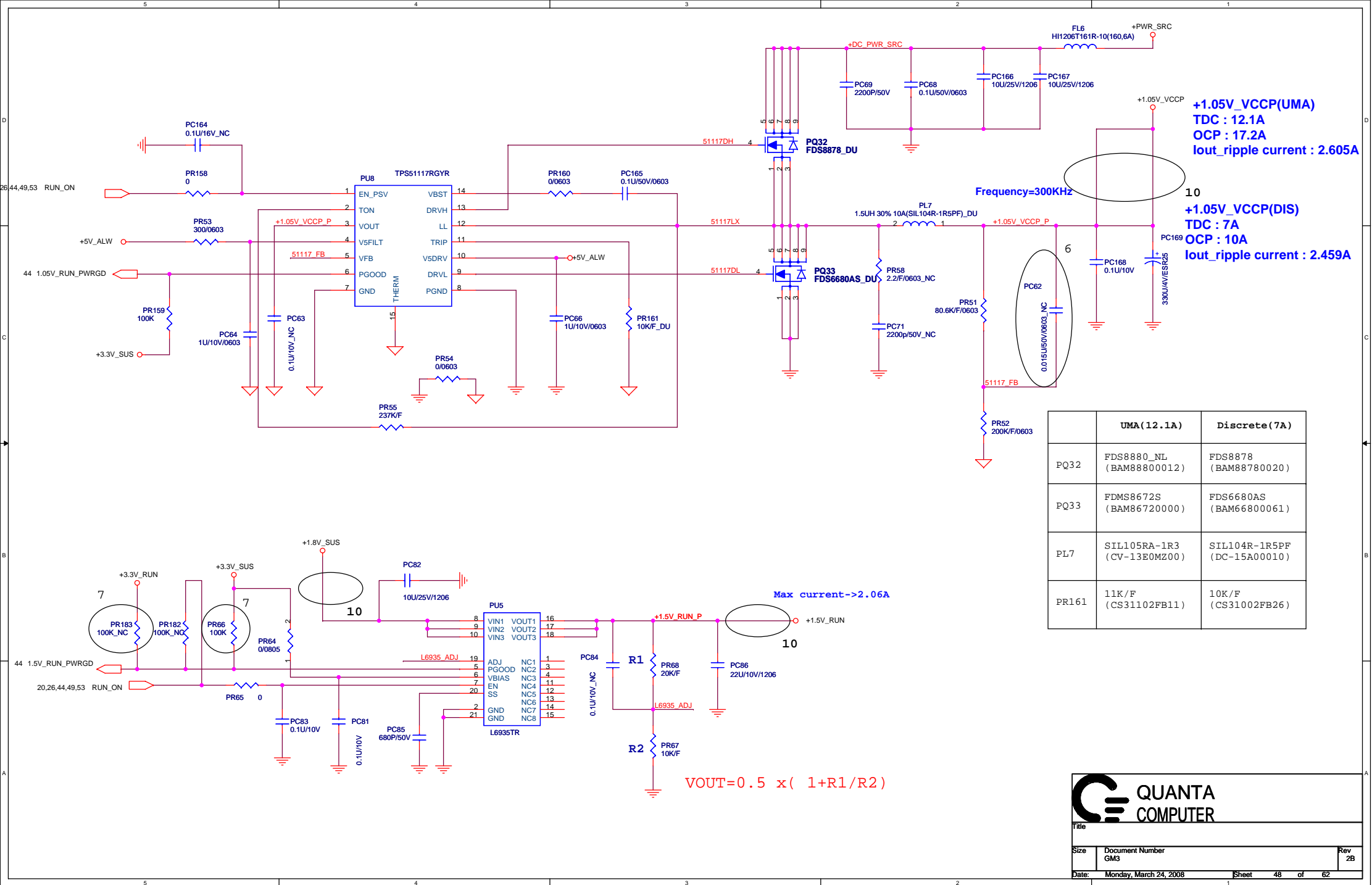


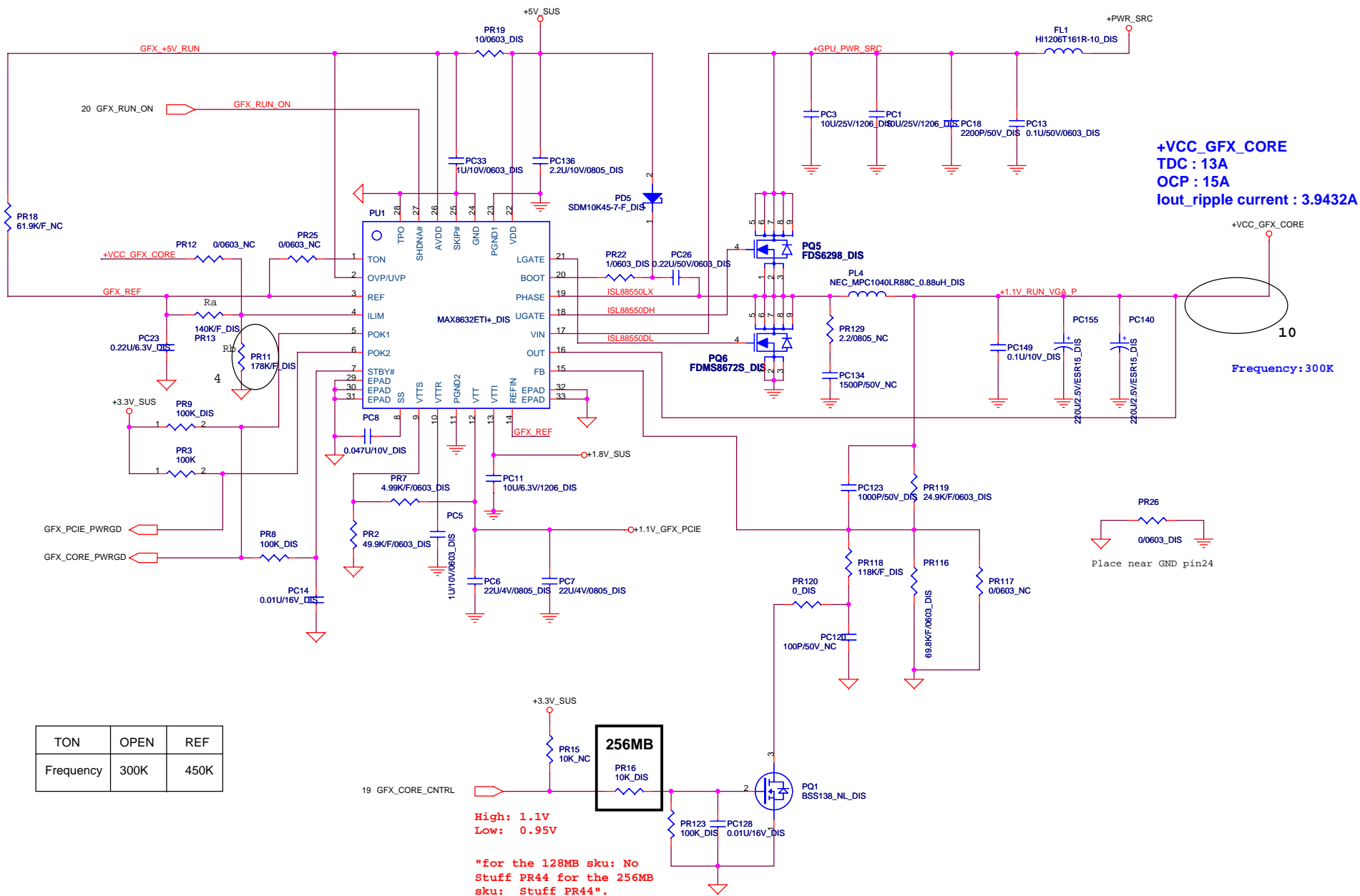
Title
Charger (ISL88731)

| Size | Document Number | Rev |
|-------|------------------------|----------------|
| GM3 | | 2B |
| Date: | Monday, March 24, 2008 | Sheet 46 of 62 |

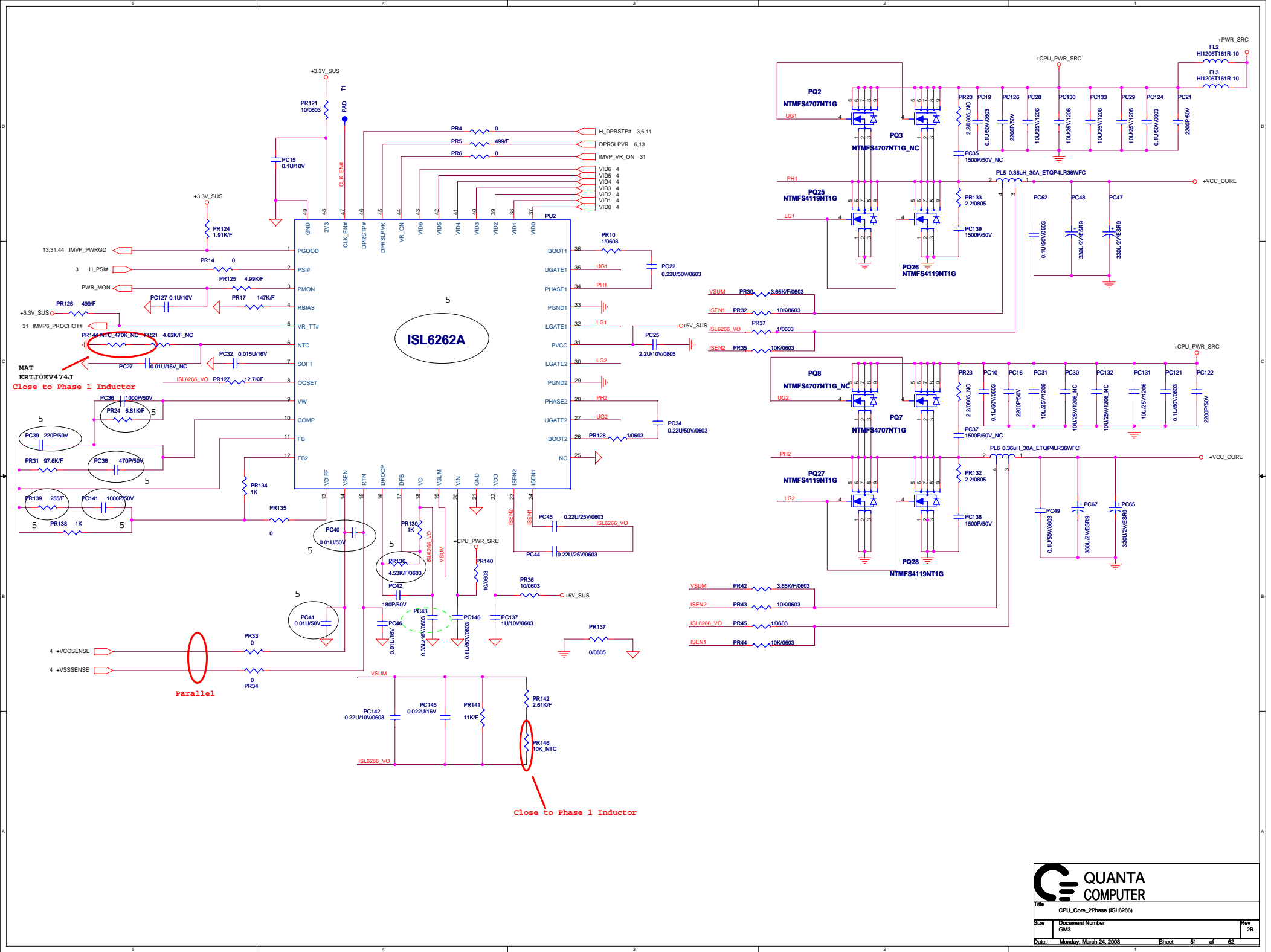
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|------------------------------------------------------------------------------------------------------------------|------------------------|----------------|
|  QUANTA COMPUTER | | |
| Title | | |
| Size | Document Number | Rev |
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| Date: | Monday, March 24, 2008 | Sheet 47 of 62 |

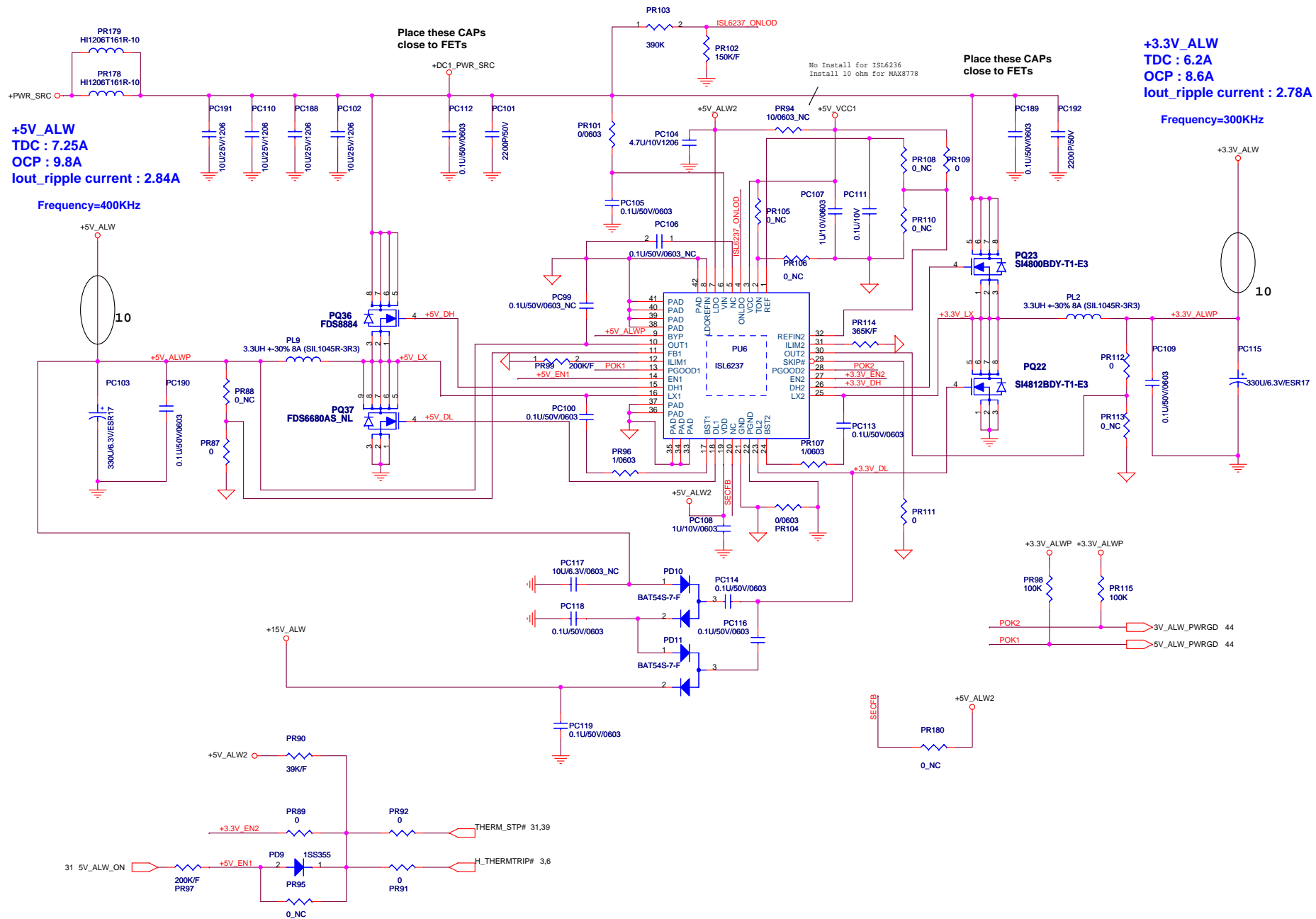


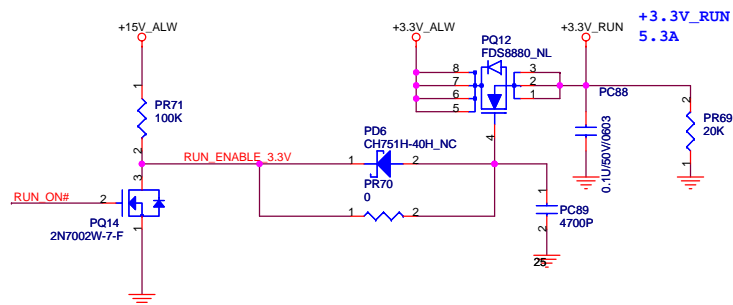
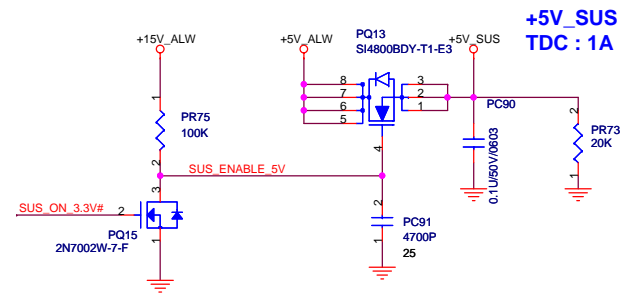
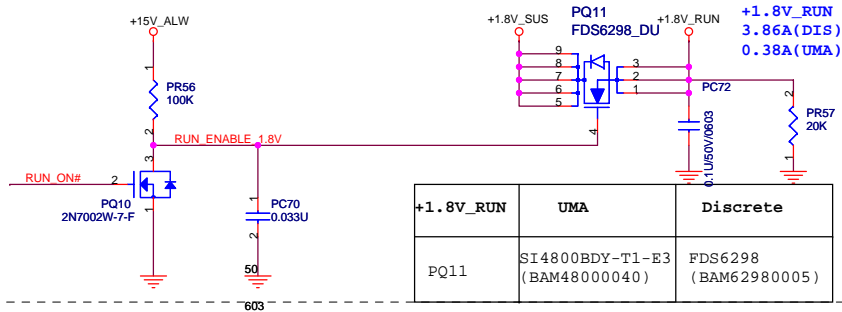
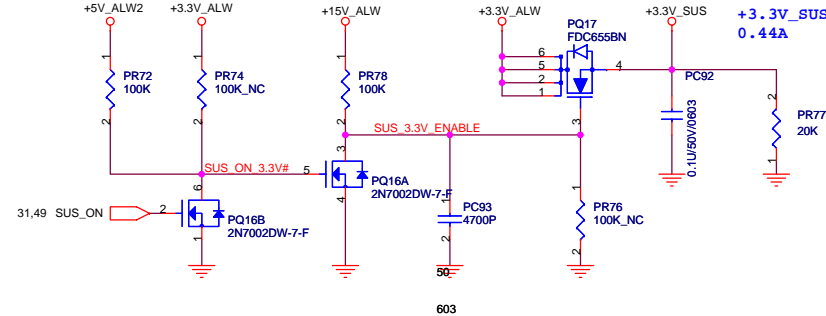
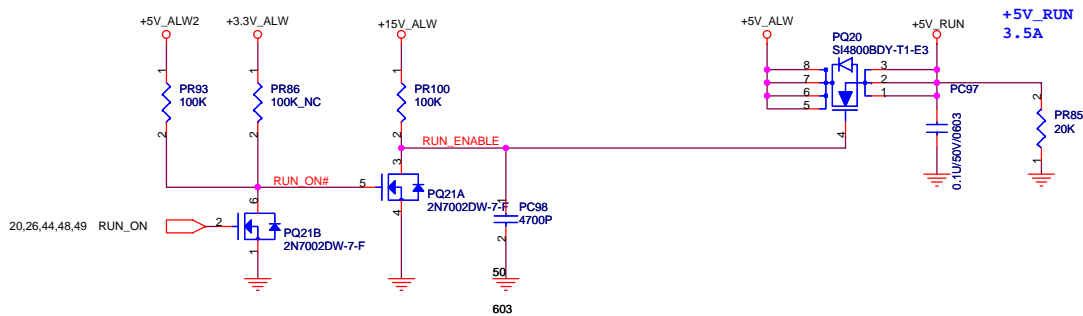


| | |
|---------|-----------------------------------------------------------------------------------|
| ILIM | $I_{ovp} = (2 * (R_b / (R_a + R_b))) * 0.1 * (1 / R_{DS(on)}) + (I_{\Delta} / 2)$ |
| SKIP# | AVDD = Low-noise, forced-PWM mode. GND = Pulse-skipping operation. |
| OVP/UVF | The overvoltage limit is 116% of Vout. The undervoltage limit is 70% of Vout. |

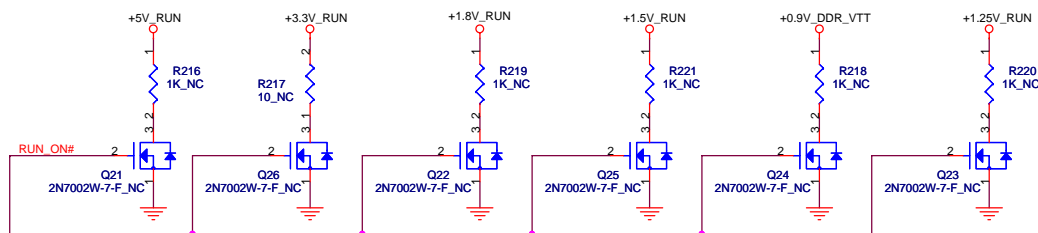


DC/DC +3V_ALW/+5V_SUS/+5V_ALW /+15V_ALW

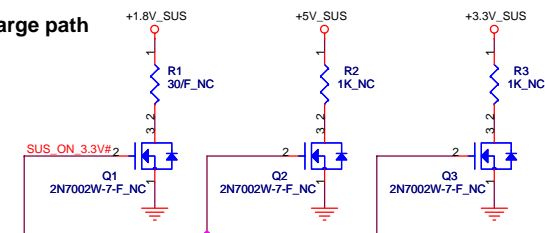




Reserve discharge path

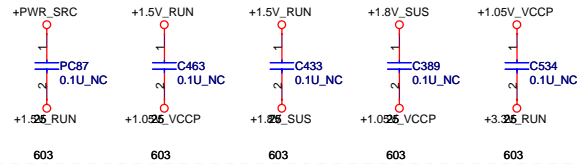


Reserve discharge path

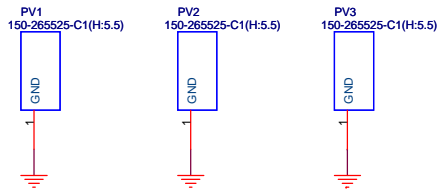


Reserved for EMI.

Stitching caps



26



Page 26
SATA (HDD&CD_ROM)

Page 27
PCCARD /CONN

Page 31
SIO(MEC5025)

Page 38
Azelia CODEC

Page 40
LAN(BCM5755M)

Page 48
1.5VRUN,1.05V(VTT)

Place C860,C216,C1426 close to PQ33.
Place C862,C222,C1427 close to PQ73.

Page 49
1.25V,1.8V,0.9V

Place C867,C254,C1428 close to PQ91.
Place C863,C253,C1429 close to PQ92.

Page 51
CPU_MAX8786(3phase)

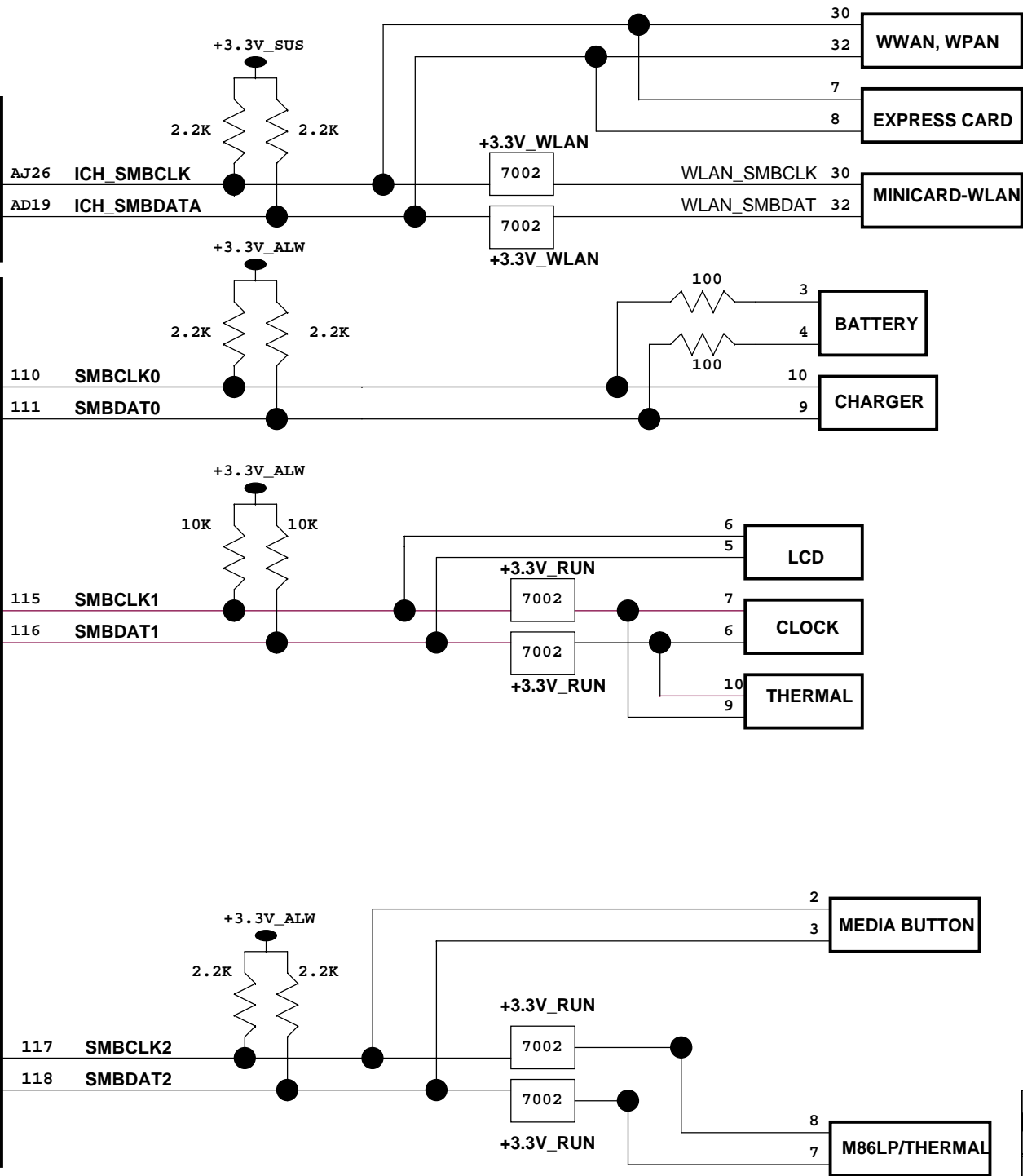
Page 52
D/D Power



| | | | |
|-------|------------------------|-------|----------|
| Title | | | EMI CAP |
| Size | Document Number | | Rev |
| | GM3 | | 2B |
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ICH8-M

SIO
ITE8512



POWER STATES

| Signal State | SLP S3# | SLP S4# | SLP S5# | S4 STATE# | ALWAYS PLANE | SUS PLANE | RUN PLANE | CLOCKS |
|------------------------------|------------|------------|------------|--------------|-----------------|--------------|--------------|--------|
| S0 (Full ON) / M0 | HIGH | HIGH | HIGH | | | | | |
| S3 (Suspend to RAM) / M1 | LOW | HIGH | HIGH | | | | | |
| S4 (Suspend to DISK) / M1 | LOW | HIGH | HIGH | | | | | |
| S5 (SOFT OFF) / M1 | LOW | HIGH | LOW | | | | | |
| S3 (Suspend to RAM) / M-OFF | LOW | HIGH | HIGH | | | | | |
| S4 (Suspend to DISK) / M-OFF | LOW | LOW | HIGH | | | | | |
| S5 (SOFT OFF) / M-OFF | LOW | LOW | LOW | | | | | |

PM TABLE

| power plane State | +3.3V_ALW +3.3V_RTC_LDO +3.3V_WLAN +5V_ALW +15V_ALW | +1.8V_SUS +1.8V_LOM +3.3V_LAN +3.3V_SUS +5V_SUS | +0.9V_DDR_VTT +1.05V_VCCP +1.25V_RUN +1.5V_CARD +1.5V_RUN +3.3V_CARD +3.3V_CARDAUX +3.3V_R5C832 +3.3V_RUN | +3.3V_RUN_CARD +2.5V_RUN +5V_MOD +5V_RUN +5V_SPK_AMP +CPU_PWR_SRC +VCC_CORE +VDDA | +DC_IN +DC_IN_SS +PWR_SRC +RTC_CELL |
|----------------------|-----------------------------------------------------------------|-------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------|----------------------------------------------|
| S0 | ON | ON | ON | | ON |
| S3 | ON | ON | OFF | | ON |
| S5 S4/AC | ON | OFF | OFF | | ON |
| S5 S4/AC don't exist | OFF | OFF | OFF | | ON |

PCI TABLE

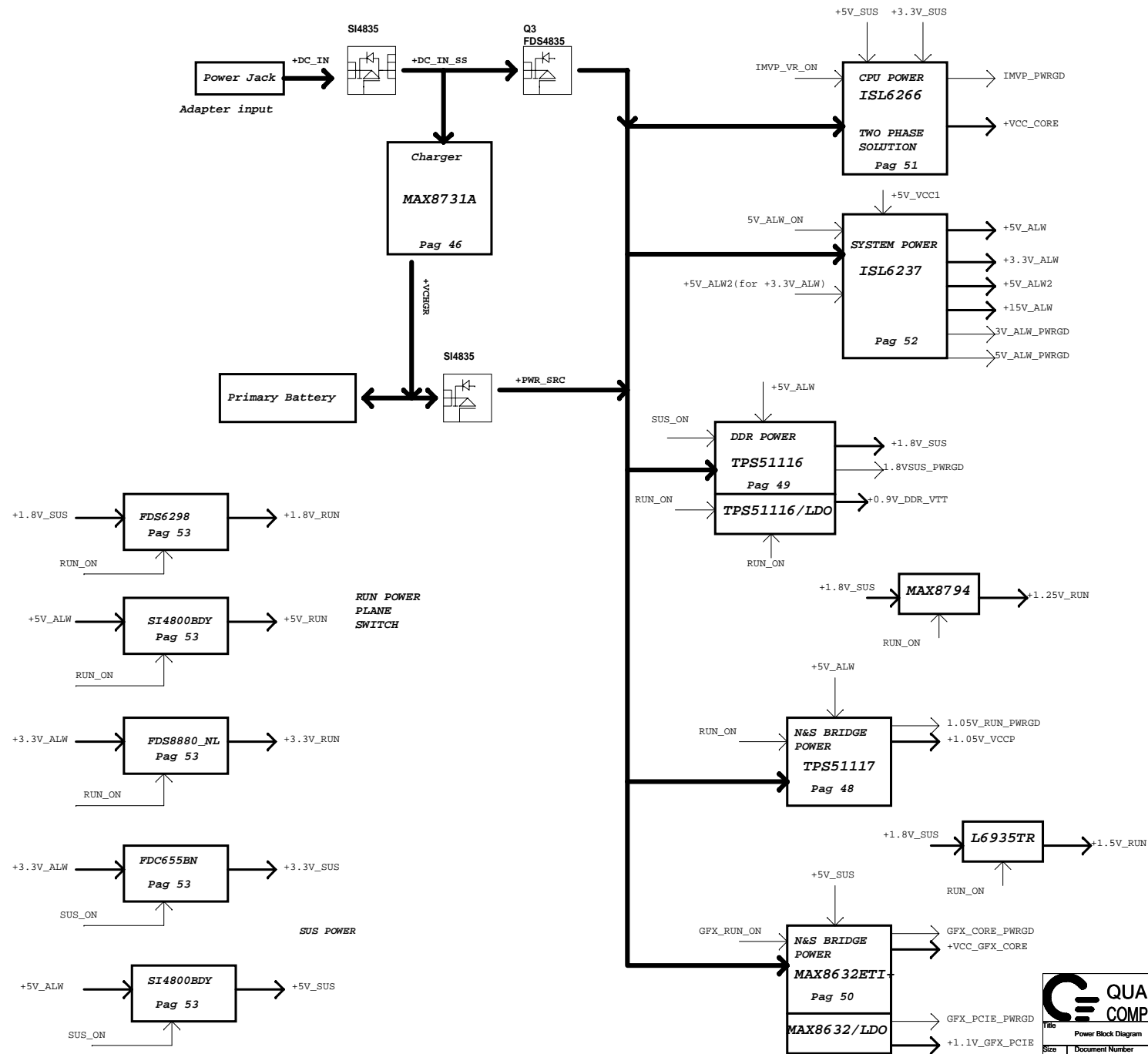
| PCI DEVICE | IDSEL | REQ#/GNT# | PIRQ |
|------------|-------|---------------|-----------------------------------|
| BCM4401B | AD16 | REQ#0 / GNT#0 | PIRQB |
| R5C833 | AD17 | REQ#1 / GNT#1 | PIRQC: Card reader PIEQD: 1394 |

| ICH8-M | USB PORT# | DESTINATION |
|----------|-----------|-----------------|
| | 0 | Right Top |
| | 1 | Right Bottom |
| | 2 | Side TOP |
| | 3 | Side Bottom |
| | 4 | Ext. USB TOP |
| | 5 | Digital Camera |
| | 6 | Express Card |
| | 7 | WPAN/Bluetooth |
| | 8 | Ext. USB Bottom |
| ECE 5011 | 9 | WWAN |
| | 1 | None |
| | 2 | None |
| | 3 | None |
| | 4 | None |

| PCI EXPRESS | DESTINATION |
|-------------|------------------|
| Lane 1 | MINI CARD-1 WWAN |
| Lane 2 | MINI CARD-2 WLAN |
| Lane 3 | MINI CARD-3 WPAN |
| Lane 4 | Express Card |
| Lane 5 | None |
| Lane 6 | None |

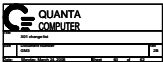
GM3 Power Design Block Diagram

2007/09/06




| Model | Page | Date | Rev | Description |
|-----------------|----------|------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Pacino of Intel | | | | |
| | 1 | AR | 725 | 1A |
| 2 | 39 | 803 | 1A | 1A2 review schematic and recommend add 0.1uF between RNM37002_3 and RNM37002_3. This is just a reservation in case there's any noise coupling issue happening. Then have 2 different filter cap location (one near RNM37002 and the other near the UTP 1804 of course. JOLY one cap can be installed). |
| 3 | 25 | 803 | 1A | 1A2 review schematic and recommend add poly switch and 0.1uF cap value to R7_408 of RNM 0086 to avoid SW reset. |
| 4 | 29 | 803 | 1A | 1A2 review schematic, R7_720 pin-vinco S203 don't need cap to GND. |
| 5 | 37 | 803 | 1A | The wiring on UTP171 is for enabling SD audio on RNM, so pull to high. |
| 6 | 54 | 803 | 1A | move the right side USB and 20-1A connector schematic to 7B, so change WTR(73) COMB to 32pin |
| 7 | 39 | 803 | 1A | R115 1A2 review schematic: reverse WMS signal for working properly. change voltage allocation resistor to make sure the input clock swing level is at 1.8V |
| 8 | 39 | 803 | 1A | R116 per USB recommend, use 7002 to avoid the leakage current from R7_203. |
| 9 | 37-38 | 807 | 1A | R117 add diode to protect below GND port pin8---PANEL_FSM pin8---DIFFERENTIAL and POWER_0H_1804, R37---RNM37002 |
| 10 | 52 | 820 | 1A | R120 For 1A2 suggestion, change pump from +5V LDO, might cause high voltage voltage. Add R118 100k 3V/003. |
| 11 | 52 | 820 | 1A | Since PDS0878 Rg too big, change RQ44 to PDS0884. |
| 12 | 52 | 820 | 1A | Change P225 to 180K and P224 to 294K for setting current limit. |
| 13 | 52 | 820 | 1A | For 1A2 recommend , R016 could be deleted. |
| 14 | 49 | 820 | 1A | Change R065 to 145K for 1.82 output voltage |
| 15 | 48 | 820 | 1A | Due to output ripple current too big ,change R125 from 0.88uH to 1.5uH. |
| 16 | 48 | 820 | 1A | R0449 should be cancelled, not necessary |
| 17 | 48 | 820 | 1A | Change R0452 to 9.09k for OCP |
| 18 | 48 | 820 | 1A | For 1A2 recommend , R0447 no stuff, reserved. |
| 19 | 48 | 820 | 1A | Add R079 for meet output ripple current. |
| 20 | 48 | 820 | 1A | Change R0122 to 4.3K and R0125 to 49.9k for setting VTP11.IV. (VTP <REFIN/2+1V) |
| 21 | 36 | 822 | 1A | Added LED level shift for support white LED need use 5V drive. |
| 22 | 22 | 823 | 1A | add level shift circuit to protect thermal IC |
| 23 | 42 | 823 | 1A | add level shift circuit to prevent ALM and LAM pin interconnect |
| 24 | 48-49 | 824 | 1A | check single net and current by JM |
| 25 | 52 | 827 | 1A | Due to S110458-1000P will be R05, change R111, R112 to S110458-363. |
| 26 | 37 | 827 | 1A | change R8 pin number to 32 pin |
| 27 | 43 | 828 | 1A | change LED of LAM jack control signal to LINELED |
| 28 | 43 | 828 | 1A | On-layout E2W card connector and WTR together |
| 29 | 37 | 828 | 1A | Will add update R10 pin define to 14 pin and re-define pin definition |
| 30 | 31 | 828 | 1A | R2014 is output pin, so change to pin 85, and R8_2078 from pin 85 change to pin 79. |
| 31 | 39 | 828 | 1A | reverse 1-4 pin definition for thermal test design |
| 32 | 26,12 | 829 | 1A | change R30813 RCT_F1Q208 to RCT_F1Q208 for AMD platform signal control requirement |
| 33 | 37 | 829 | 1A | Due to more keyboard light sensor to media button board, add R8_2007179_207 function to media button connector pin 10. |
| 34 | 37 | 829 | 1A | change keyboard pin number to 32 pin |
| 35 | 48 | 829 | 1A | For 1A1 recommend ,change 1.5V LDO from RNM3704 to ST L6935. |
| 36 | 49 | 829 | 1A | For V1 1A2 recommend ,connect R074 to GND. |
| 37 | 35 | 830 | 1A | For support power USB function, change power to +V_ALM |
| 38 | 31 | 830 | 1A | change DIFF_F1Q20079 firm pin 88 to GPT 1 for design requirement , and pin88 margin to +V_ALM_0H |
| 39 | 25,43,38 | 830 | 1A | For EMC test requirement , reserve cap, R20 protect, common choke at COM side |
| 40 | 52 | 830 | 1A | Add R0180 for reserve RNM3779 IC. |
| 41 | 52 | 830 | 1A | Due to Farina need to support USB charger function,change following item. 1.Change power pin from +V_ALM to +V_ALM2 pin . pin7 pin118, R0118 and R0116 2.Add a load switch RQ42 for +V_ALM to +V_ALM2 |
| 42 | 26 | 831 | 1A | refer RNM platform, change to 100 uH |
| 43 | 22 | 90 | 1A | Reserve external spread spectrum circuit for ATI graphic using |
| 44 | 48 | 90 | 1A | change R0455 to 237K from 178K to setting switching operating frequency at around 300 KHz |
| 45 | 52 | 90 | 1A | For 1A2 recommend, change R014 input power from "+V_ALM2" to "+V_ALM" and R0118 can be 0k. |
| 46 | 52 | 90 | 1A | For 1A2 recommend, connect pin20 to pin19 for L1E218 (or RNM3778) can populate on L1E217 location. |
| 47 | 49 | 90 | 1A | Change R0155 to correct net name "+1.8V_R03_P". |
| 48 | 29 | 90 | 1A | RNM internal thermal protect function pin is high active, re-design protect logic circuit for it. |
| 49 | 54 | 90 | 1A | For EMC requirement , add Reserve on jump on +VTRM and close to pin1 and 2 of J40RT1 |
| 50 | 35 | 90 | 1A | Reserve ESD protector at J4 pin1 (+V_R03) for Biometric (close to J4) |
| 51 | 48 | 90 | 1A | Add R079 for reserve debug noise issue. |
| 52 | 48 | 90 | 1A | Change R05 pin through PDS8 to +3.3V_R03. |
| 53 | 49 | 90 | 1A | Change R079 from 10K to 0ohm. |
| 54 | 59 | 90 | 1A | For reserve RMI number, add R0117 and R0117. |
| 55 | 48 | 90 | 1A | For 1A11 recommend , reserve R0143 and R0144 for V1 controller. |
| 56 | 38 | 90 | 1A | For 1A11 recommend , Add GND pin to mark R02 and R7 LED active |
| 57 | 27,33,34 | 90 | 1A | For LAM card using CSE-800 pin, so change CSE_P0TE_R001 to RNM and CSE_P0TE_R001 to RNM. |
| 58 | 26,6 | 90 | 1A | add 1000K pair 1000 signal to support 24bit panel |
| 59 | 31 | 94 | 1A | delete JCKV_L02_2079 pin for DC jack design, so move R2014 to pin79. |
| 60 | 46 | 90 | 1A | Reserve a 0.0H R055 resistor for SA test. |
| 61 | 46 | 90 | 1A | Add R0145 for ST 1A2 recommend. |
| 62 | 37 | 96 | 1A | Add R8_2007179_207 control circuit on RM side |
| 63 | 37 | 96 | 1A | Add L_ALM at pin 5 for L02 switch IC power pin |
| 64 | 42 | 96 | 1A | Reserve RNM704K 0008_1000 circuit. |
| 65 | 39 | 98 | 1A | Add RMC card function at card reader connector |

| Model | Item | Page | Date | Rev. | Description |
|-----------------|------|------------------|-------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Pacino of Intel | 1 | 12,13, 17,21, 59 | 9/27 | 2A | modify SBT design issue! 1. delete unnecessary 0 ohm resistor 2. adjust current for program for D10/DA(R511a142) 3. Change CLK_PWDN pull high 4. PWDN_SLEEP pull down to avoid floating. 5. NC R451 to set Boot BIOS Strap for LPC Interface |
| | 2 | 52, 50 | 10/2 | 2A | For second source concern, change below item. 1. Change P09 from R4814 to 10K155 2. Change P09 from C0810-40PF to E0410245-7-F 3. Change PQ1 from R05118-7-F to R05118_RL |
| | 3 | 8 | 10/3 | 2A | use 0R05 0 ohm to instead of jump1/RW, 1.6A per resistor) |
| | 4 | 19 | 10/3 | 2A | pull high the GPIO 0 & GPIO 1 to enable PCIe PULL TX OUTPUT DRING and PCIe TRANSMITTER DE-SERIALIZED function to solve no display problem. |
| | 5 | 41 | 10/15 | 2A | The camera pin assignment changed ! 2 pin camera power pin and they are 3.3 V .. |
| | 6 | 40 | 10/16 | 2A | change resistor setting for STA920073C chip |
| | 7 | 46, 52 | 10/15 | 2A | Due to SI48100DY-T1-E3 will be EOL, change PQ29 and PQ22 from SI4810 to SI4812. |
| | 8 | 19 | 10/16 | 2A | Due to VDD04 and VDD05(option reference source voltage) use 1.8V_R0M, FMS suggest OFFDATA use 1.8V pull high |
| | 9 | 33 | 10/17 | 2A | remove external SIM card CONN that on MB side |
| | 10 | 13 | 10/17 | 2A | It is multi function pin(SMBALESTW/DFD011). Before bios programming, the STM function is SMBALEST. If it is pull high to 3.3V_R0M, the SCH will be alert by this pin. It cause the ST can't normally sleep when system could boot first time. so change to SUS power |
| | 11 | 38 | 10/18 | 2A | Sniffer behavior is reverse, so modify design at PT stage |
| | 12 | 42 | 10/18 | 2A | change to 5784 design |
| | 13 | 40 | 10/22 | 2A | change TP46040A4 symbol design to meet SPEC definition |
| | 14 | 19 | 10/22 | 2A | FMS suggest: Ground P10/S10/R10 and Implement P10ST to GND even if DMC2 is unused. |
| | 15 | 43 | 10/23 | 2A | for factory requirement---increase pad length for SMT yield rate |
| | 16 | 41 | 10/24 | 2A | for DELL SPEC---change camera conn pin definition |
| | 17 | 31, 37 | 10/25 | 2A | modify LED Key board illumination schematic and remove EC pin 68 |
| reserve | 18 | 44 | 10/28 | 2A | HWFG monitor change: change 3V/5V_ALM_PWDN to GPF_PCIE/COSE_PWDN |
| reserve | 19 | 12,13, 14,31 | 10/29 | 2A | create +3.3V_S5 and +5V_S5 power at ICH part to fix ITE chip SUS resume problem, and move L10_SW to pin148 and pin 120 for S10M using |
| | 20 | 35 | 10/30 | 2A | add PWDN1492 to control USB signal can be passed above SUS, and USB_S10M_R09 can control whether USB can supply power for external device at RS mode |
| reserve | 21 | 53 | 10/30 | 2A | For EE request , add two power rail '+3.3V_S5' and '+5V_S5' for south-bridge battery mode. |
| | 22 | 48 | 10/30 | 2A | 1.5V_R0M_PWDN pull-high to R0M_ON for solve glitch issue. |
| | 23 | 16,54 | 10/30 | 2A | add 1000p cap and close to connector for EMI |
| | 24 | 35 | 10/30 | 2A | change LCP connector pin definition for LED panel! 1. change pin 8 from GND to +5V_ALM 2. change pin 16 from GND to LCP_VCC |
| | 25 | 31 | 11/1 | 2A | change GPIO design 1. delete pin 83 SNIPPER_YELLOW 2. move 5V_ALM_ON to pin 83 3. swap pin 108 WIRELESS_ON/OFF and pin 35 SNIPPER_PWR_SW |
| | 26 | 38 | 11/1 | 2A | change GPIO design 1. swap WIRELESS_ON/OFF and SNIPPER_PWR_SW 2. reserve SWIPF100/PFEL_YELLOW |
| | 27 | 31 | 11/5 | 2A | change GPIO design for fix thermal no function issue 1. NC ADAPT_OC and ADAPT_TRIP_SEL 2. add 5V_ALM_ON function at pin 76 |
| | 28 | 3 | 11/5 | 2A | Modify H_THERMTRIP9 Voltage Level shift circuit. |
| | 29 | 41 | 11/6 | 2A | add one GND pin for Audio precision 48 value |
| reserve | 30 | 37 | 11/8 | 2A | add circuit to control CIR power |
| | 31 | 49 | 11/12 | 2A | Add PR181 for reserve +5V_ALM2. |
| | 32 | 43 | 11/12 | 2A | for EMI requirement, add 7p cap close to LAN switch |
| | 33 | 37 | 11/13 | 2A | for DELL requirement, add fuse between +5V_R0M and WR_LED |
| | 34 | 31 | 11/13 | 2A | use pin 14(MD27F) to monitor THERM_STP# Function |
| | 35 | 25 | 11/13 | 2A | for Silicon image FMS suggestion! 1. EMI may come from the impedance mis-match, that'll get distorted waveform . Try to replace the common choke with (i.e 22 ohm) resistor. 2. Try to reduce the source termination resistor (i.e 300 ohm -> 150 ohm) to get cleaner eye . 3. change AVCC33V to 3.3V_R0M |
| | 36 | 25 | 11/13 | 2A | per FMS suggestion-change C313 and C314 to 2.2n for better Audio precision |
| | 37 | 50 | 11/13 | 2A | Change PR11 to 100kOhm for set correct O.C.P. |
| | 38 | 50 | 11/13 | 2A | For EE request, set VGA voltage to 0.95V/1.1V. Change PR116 to 69.8K and PR118 to 118K. |
| | 39 | 4 | 11/13 | 2A | Base on acoustic team test ,add two EC-cap for noise issue, Stuff C733 and C766. |
| | 40 | 52 | 11/13 | 2A | Base on test result, change PR114 to 294K for set OCP. |
| | 41 | 48 | 11/13 | 2A | Change PR161 to 11K for set correct OCP. |
| | 42 | 48 | 11/13 | 2A | For 1.05V jitter issue, change below item. DMA1 Change output CAP from 3500/2.0V/RSR10 to 3300/4V/RSR25 Discrete: 1. Change output CAP from 3500/2.0V/RSR10 to 3300/4V/RSR25 2. Add P062 1500pf |
| | 43 | 48 | 11/13 | 2A | Change 1.05V DMA P063 from PDS6676A2 to PDS66722 for improve efficiency. |
| | 44 | 49 | 11/13 | 2A | Base on EA report test , stuff PR171 and PC180 for reduce high wide VDS ring. |
| | 45 | 48 | 11/13 | 2A | Due to software support UL function via "IIMP", no stuff UL circuit. |
| | 46 | 13 | 11/14 | 2A | add 4.7k on PCIe_MCARD1_DET# trace to solve WLAN card detect issue |
| | 47 | 19 | 11/15 | 2A | change GPIO pin from 3.3V_R0M to 3.3V_delay to solve leakage problem between 3.3V_R0M and 3.3V_delay[see] when boot. |



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| Pacino of Intel | 1 | 32 | 11/26 | 2B | Change RTC connector because ME modifyr. |
| | 2 | 31 | 11/26 | 2B | Exchange 'SNIFFER_PWR_SW#' AND 'WIRELESS_ON/OFF#. per EC limitation. |
| | 3 | 31 | 11/26 | 2B | Change NUM_LED# from SIO pin98 to pin 88 and used Pin 98 for BID only per EC limitation. |
| | 4 | 54 | 11/26 | 2B | Change PSID relation parts to +5V_ALW2 for power saving in S5. |
| | 5 | 38 | 11/26 | 2B | Change Sniffer Switch power rail from RUN plane to ALW plane. |
| | 6 | 43 | 11/26 | 2B | Added LINK1000# for BCM cann't support GLAN LED driven by LINKLED#/SPD100LED#. |
| | 7 | 45 | 11/27 | 2B | Modify Screw hole base on ME update. |
| | 8 | 17 | 11/29 | 2B | Link to MCH DPLL clock is wrong. Change to correct link. |
| | 9 | 31 | 11/30 | 2B | Fine tune GPIO define for EC. |
| | 10 | 37 | 12/04 | 2B | Change MMB LED power source from 5V_ALW2 plane to 5V_ALW for power saving and avoid LED flash when AC in. |
| | 11 | 22 | 12/04 | 2B | Check AMD +3.3V_DELAY power plane connection component for AMD new update REF133-7 file. |
| | 12 | 40 | 12/19 | 2B | Change Audio AMP thermal PAD leave to NC. |
| | 13 | 31 | 12/26 | 2B | Change SMBus pull hihg resistor form 2.2k to 10k for LED panel flash. |
| | 14 | 37 | 12/26 | 2B | since we will use WLAN and BT LED to show function at factory side. Change power supply of Cap and Num LED from 5V_ALW2, 3.3V_ALW to 5V_RUN and 3.3V_RUN. |
| | 15 | 19 | 12/26 | 2B | Change HDMI detect circuit to solve external panel feed back voltage shortage then caude ATI chip can't switch to HMDI mode problem. |
| | 16 | 37 | 12/26 | 2B | Change the Media board power from 3V_ALW to 5V_ALW2 to solve LED flash issue when AC/Bat plug in. |
| | 17 | 37 | 12/26 | 2B | Change the lid switch IC power source from 3.3V_SUS to 3.3V_ALW to avoid system can enter S4 mode but wake up fail problem |
| | 18 | 48 | 1/3 | 2B | Change PC85 to 680P for meet sequence. |
| | 19 | 50 | 1/3 | 2B | Change PR7 to 4.99K for adjust +1.1V_GFX_PCIE rail. |
| | 20 | 53 | 1/3 | 2B | Change PQ11 from S08 to power package footprint. |
| | 21 | 48 49 50 52 | 1/3 | 2B | Change PR161 ,PR172 ,PR11 ,PR114 to correct resistance for reliability request. |
| | 22 | 35 | 1/4 | 2B | remove USB charge circuit |
| | 23 | 26 | 1/7 | 2B | pull DPST signal to high for setting 100% duty cycle |
| | 24 | 31 | 1/7 | 2B | pin12 should reserve 1u cap for ITE8512JX using |
| | 25 | 19 | 1/7 | 2B | modify HDMI detect circuit to fix the monitor detection problem.. |
| | 26 | 55 | 1/7 | 2B | create EMI spring |
| | 27 | 31 | 1/11 | 2B | per TXC report, we should change W1 cap to 18p |
| | 28 | 41 | 1/11 | 2B | per IDT FAE suggestion, serial 22 ohm on DMIC_CLK can help DMIC performance |
| | 29 | 37 | 1/11 | 2B | add 10u cap at JMB1, let 3.3V_ALE get lower drop voltage on MMB side. |
| | 30 | 6, 19 | 1/11 | 2B | EMI demand add 33p cap on RGB signal. |
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| Pacino of Intel | 1 | 25 | 2/14 | 3A | add level shift to separate the data and CLK of VGA IC and HDMI TV, and also reduce stray capacitance. |
| | 2 | 25 | 2/14 | 3A | change diode to reduce stray capacitance per WPI suggestion |
| | 3 | 12,28,31 | 2/14 | 3A | use pin-22 monitor ICH_AZ_CODEEC_RST# to delay NB_MUTE# signal for solve PO noise issue |
| | 4 | 50 | 2/20 | 3A | For Reliability calculate , change PR11 from 150K to 178K. |
| | 5 | 51 | 2/20 | 3A | Due to C4E hung up issue, change v_core power IC from ISL6266A to ISL6262A. Below is change list. 1. PU2: Change PN from AL006266000 to AL006262025 2. PR24: Change PN from CS28252FB15 to CS26812FB13 3. PC39: Change PN from CH11006JB18 to CH12206KB14 4. PC38: Change PN from CH12704JB07 to CH14706KB18 5. PR139: Change PN from CS11002JB32 to CS12552FB18 6. PC141: Change PN from CH22206KB16 to CH21006JB10 7. PC40,PC41: Change PN from CH1336K1B02 to CH31006KB18 8. PR136: Change PN from CS23833F911 to CS24533F921 |
| | 6 | 48 | 2/20 | 3A | For 1.05V OVP issue in Vista , no stuff PC62. |
| | 7 | 25 | 2/20 | 3A | Due to L6935 has improved powergood issue, no stuff PR183 and stuff PR66. |
| | 8 | 48 | 2/15 | 3A | add HDMI solution per Silicon image suggestion 1. Change R233 to 650 ohm 2. Remove external RC between HDMI +/- signal. add HDMI EMI solution DIS:CXCG900U000 / EXC24CG900U; UMACXCXG240U000 / EXC24CG240U |
| | 9 | 35 | 2/23 | 3A | add common chock for EMI solution Quanta PN: DC09004A014 |
| | 10 | 35 | 2/25 | 3A | cange power jump to 0805 resistor |
| | 11 | 27 | 2/25 | 3A | add filter CAP for EMI |
| | 12 | 13, 37 | 2/25 | 3A | by ICH-8 GPIO-17 dectect the LED keyboard connector |
| | 13 | 17 | 2/26 | 3A | exchange 27SS and 27NSS / DREF_SSCLK# & DREF_SSCLK for follow CLK GEN spec. design. |
| | 14 | 13 | 2/27 | 3A | ICH_RSMRST# pull down for RTC timer issue when plug in AC |
| | 15 | 40, 41 | 2/27 | 3A | MUST ADD 2.2K-OHM RESISTORS TO PREVENT AMPLIFIER CLIPPING and ADD 220PF CAPACITORS TO ALLOW PROPER DYNAMIC RANGE MEASUREMENTS |
| | 16 | 19 | 22/29 | 3A | Add 10k ohm on HDMI_DET to ensure Vin on test fixture input 2.4V the voltage not drop under 2V spec. definition. |
| | 17 | 9 | 03/03 | 3A | Based on SR_check 1.6, UMA should pull down 75 ohm on TV_DAC pins if disable TV-out function. |
| | 18 | 40 | 03/05 | 3A | Change C518, C519 from 0.033uF to 0.01uF per Dell audio update requirement. |
| | 19 | 40 | 03/20 | 3A | Change net name of "AUD_HP2_L1" between R708 & C525 to "AUD_HP2_L0_R" and "AUD_HP2_R1" between R708 & C525 to "AUD_HP2_R0_R" for the original net name same as U20.15 & U20.16 will cause the HP2 no function. |
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| | | | | | <div><div><div>QUANTA COMPUTER</div></div><div><div><div>Title</div><div>A00 change list</div></div><div><div><div>Size</div><div>Document Number</div></div><div><div>GM3</div><div>Rev</div></div></div><div><div><div>Date</div><div>Monday, March 24, 2008</div></div><div><div>Sheet</div><div>62 of 62</div></div></div></div></div> |

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